OPAL-RT Bootcamp

Overview of Hardware and Opal-RT Simulator

The What & Why of Real-Time Simulation

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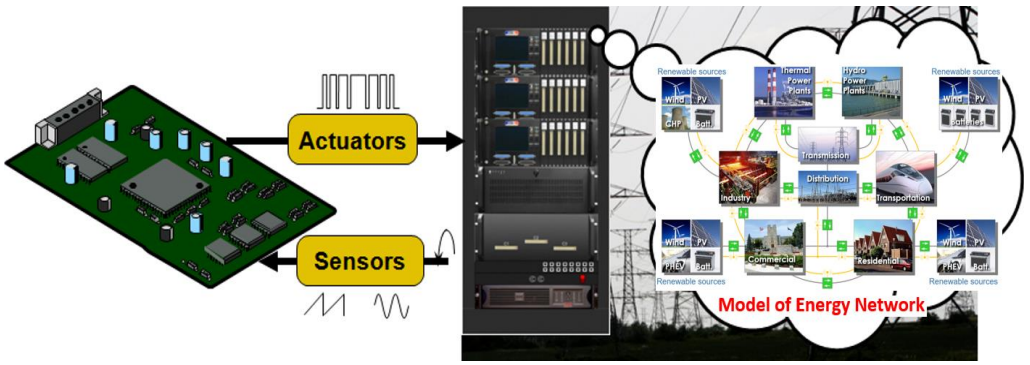
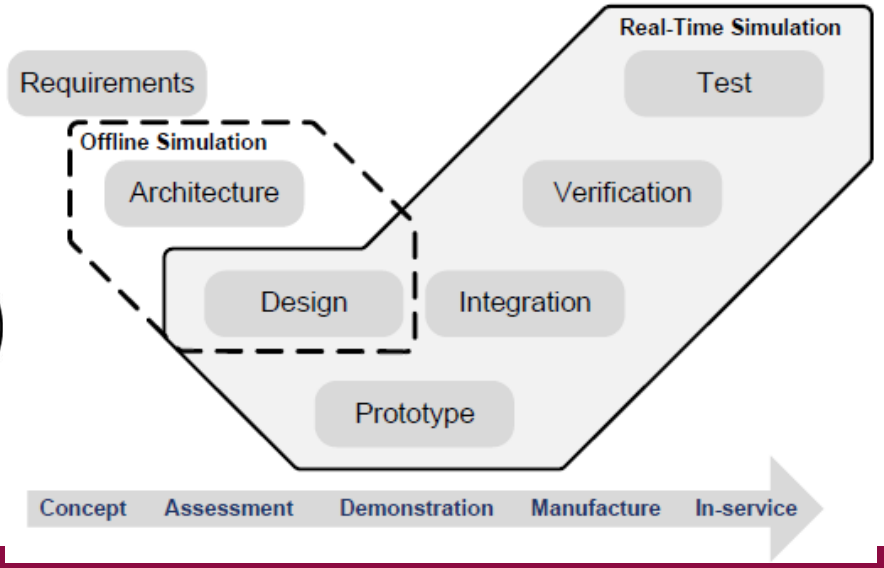
Skill Development

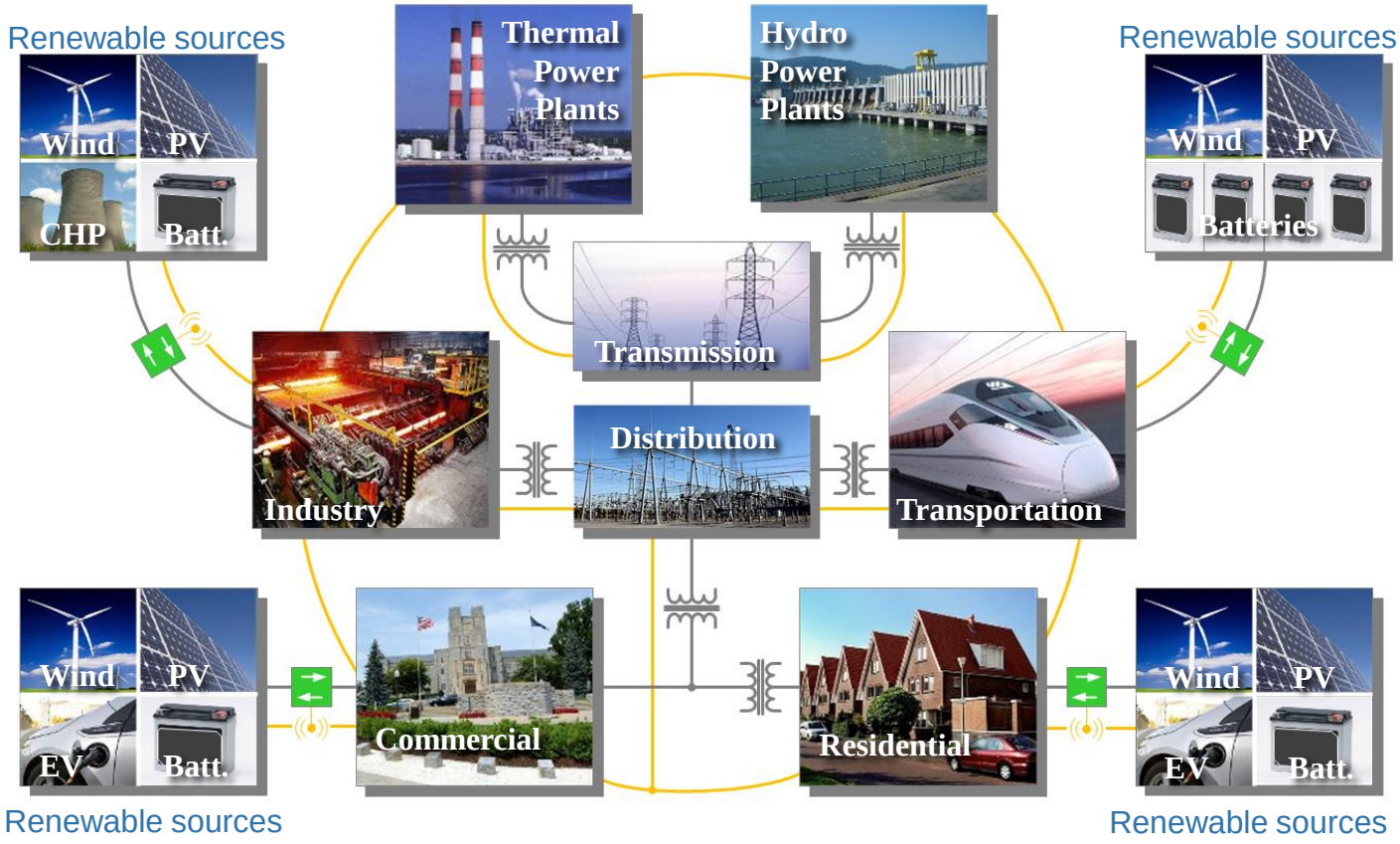
Integrated basic education/principles and skills training

- Education with skills that are sure to be needed in the coming years!
- **Real-time models present a fair and accurate method for assessing issues**
- **Providing clear resolutions to the sustainable energy developers, utilities, etc.**





“Smart Grid”



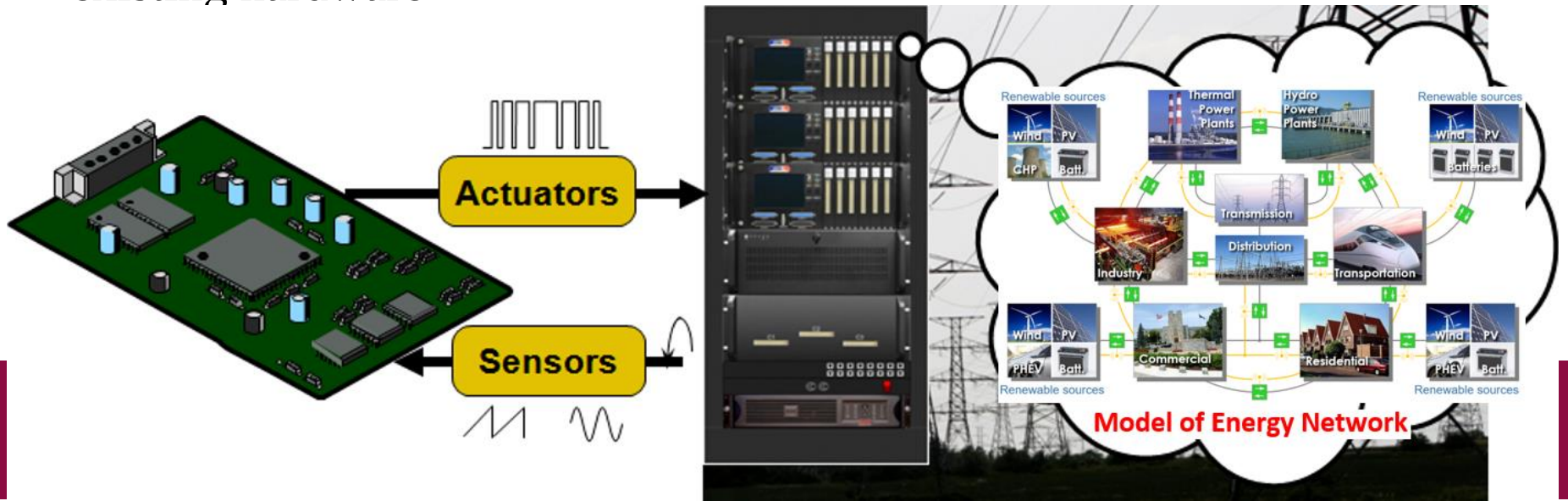
Integrated of Electrical & Information Infrastructures… securely !

Smart Network with wireless communication system for energy management

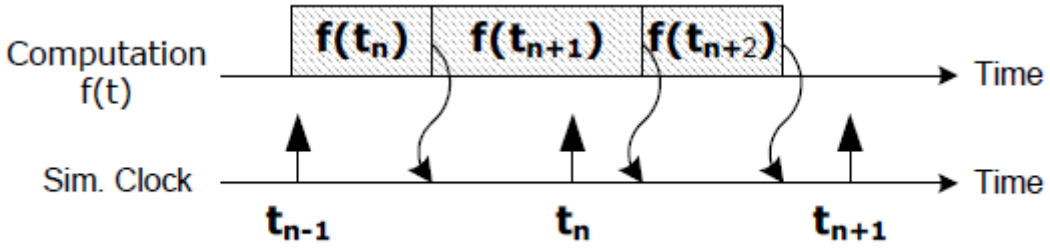
Contribution of Real-Time Simulation

- **Purpose:**
  - RT testing to accurately produce the simulation outputs within the same lengths of time in its physical counterpart
  - Replace real-hardware by a Real-Time model

- Allows destructive test, Discover Design Issues Earlier in the Process
- Reducing development costs, replace risky/expensive tests on none-existing hardware

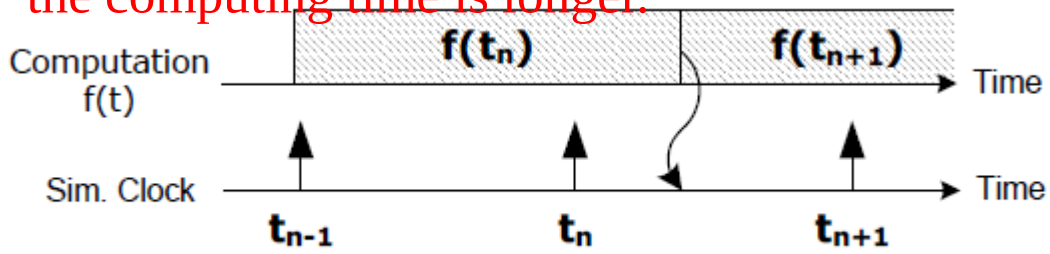


Real-Time Simulation Requisites and Other Simulation Techniques

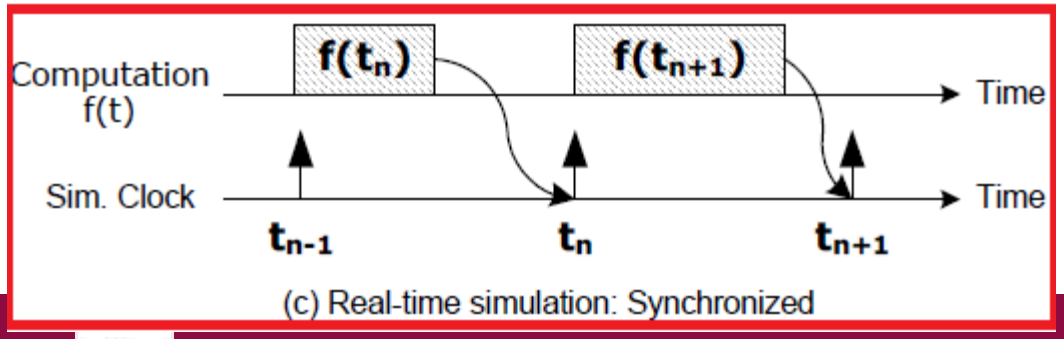


(a) Offline simulation: Faster then real-time

the computing time is longer.



(b) Offline simulation: Slower then real-time

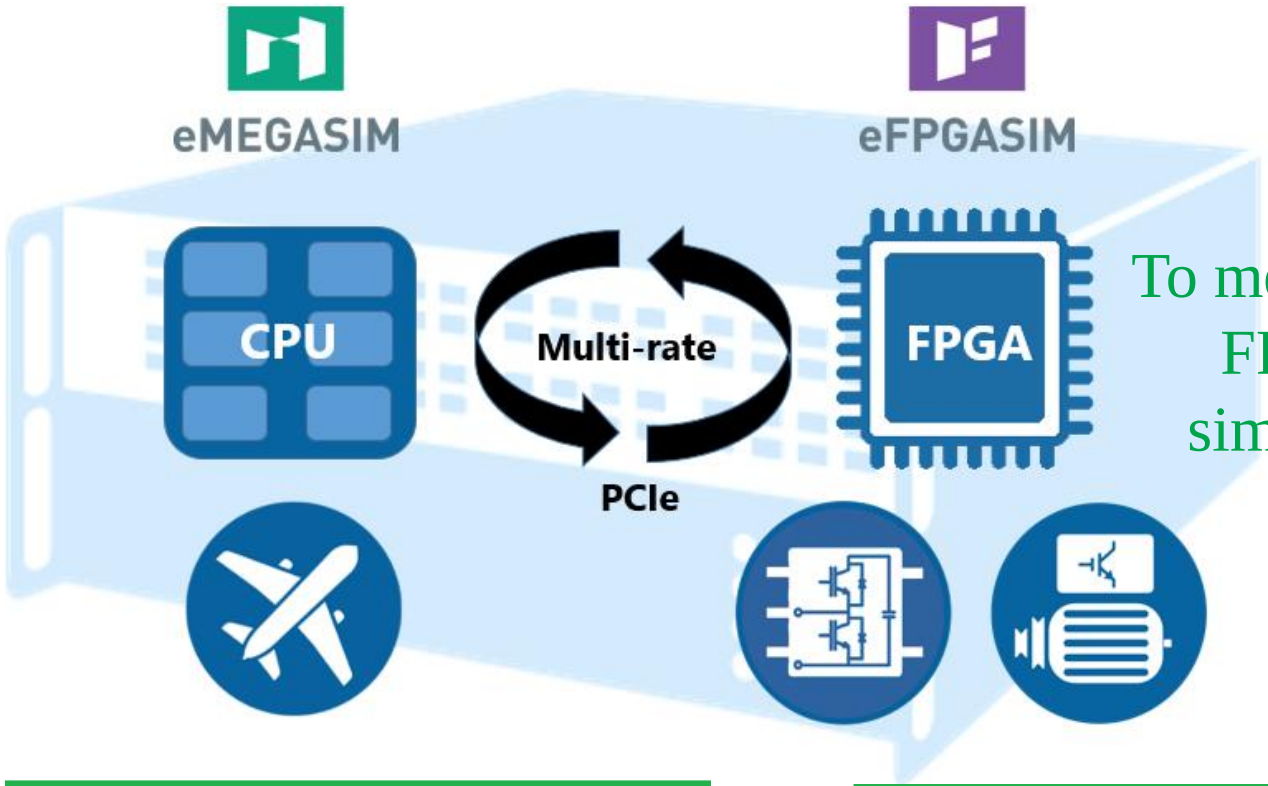


(c) Real-time simulation: Synchronized

To solve mathematical functions/equations at a given time-step, each variable or system state is solved successively as a function of variables and states at the end of the preceding time step.

Accurately produce the internal variables/outputs of the simulation within the same time length that its physical counterpart would.

Combine Simulation Systems



To meet timing requirements, FPGA-based real-time simulation is an effective solution.

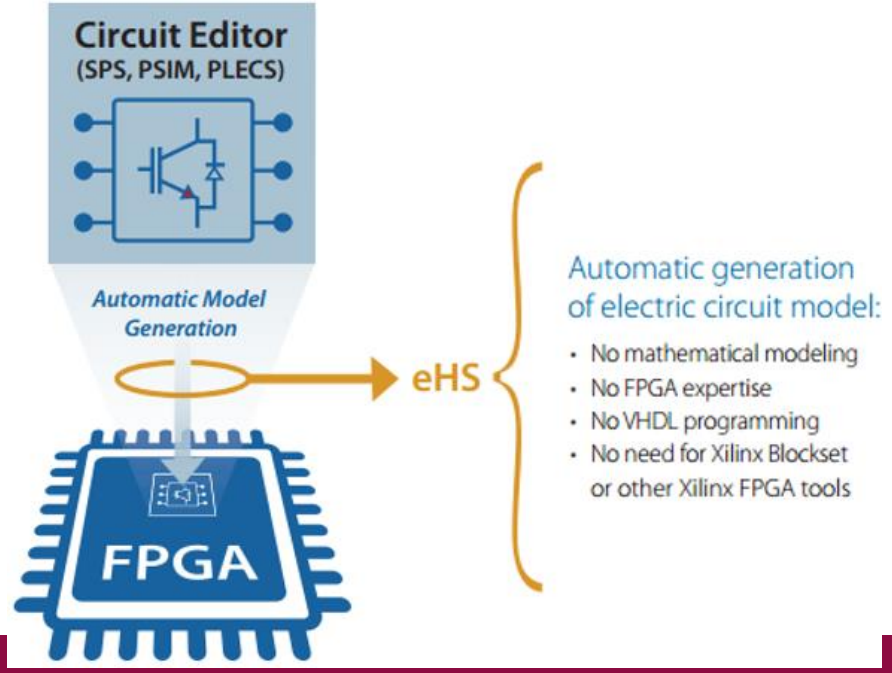
CPU model - mechanical, dyamics, control (Ts~20 µs)

FPGA model – electronics, motors (Ts< 1 µs)

But : implementing and solving differential equations on FPGA is tricky and requires advanced FPGA programming skills.

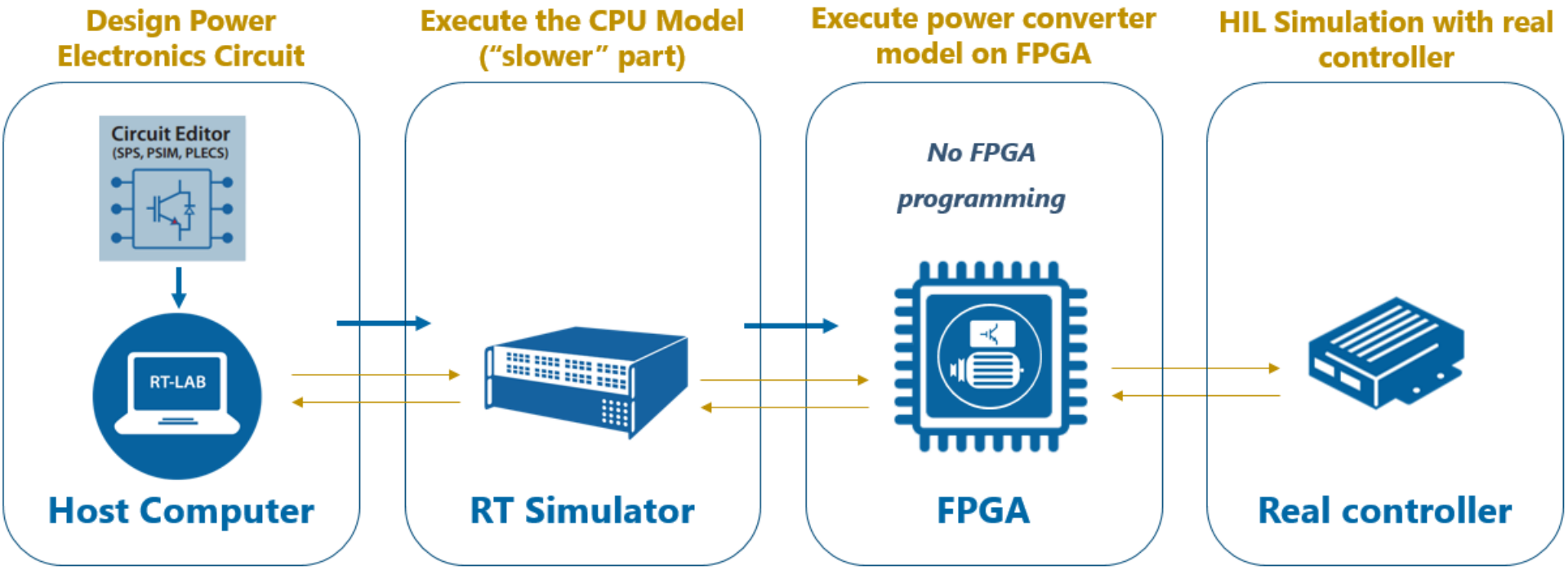
Contribution of Real-Time Simulation

- eHS: electrical Hardware Solver
- Allows the use of a comprehensive circuit editor
- and taking advantage of the FPGA performance
- without writing a single line of HDL code !



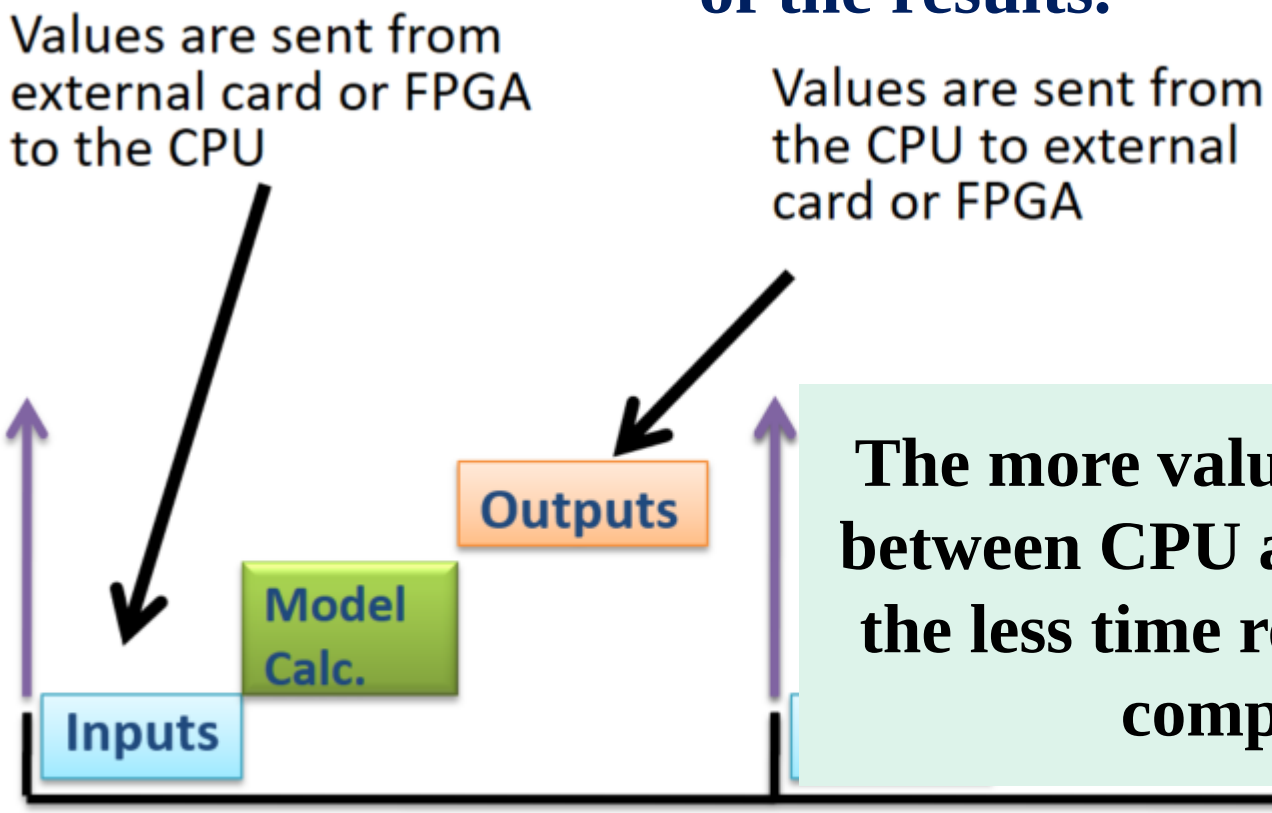
Real-Time HIL Simulation

- Workflow



Contribution of Real-Time Simulation

Having a small time-step on FPGA increases the accuracy of the results.



The more values are exchanged between CPU and external card, the less time remains for model computation!

OP5600 Hardware Overview

- There are multiple hardware platforms!
- **Main features:**

- Powerful real-time target with up to 12 INTEL processor cores 3.3 GHz
- Real-time operating system : QNX or Linux REDHAT
- Xilinx SPARTAN 3 or VIRTEX 6 FPGA

- Up to 128 analog I/O or 256 digital I/O or a mix of both
- Rear DB37 connectors
- Front I/O monitoring (access to all I/Os)
- Up to 4 PCI slots

- **Support for third-party I/Os**

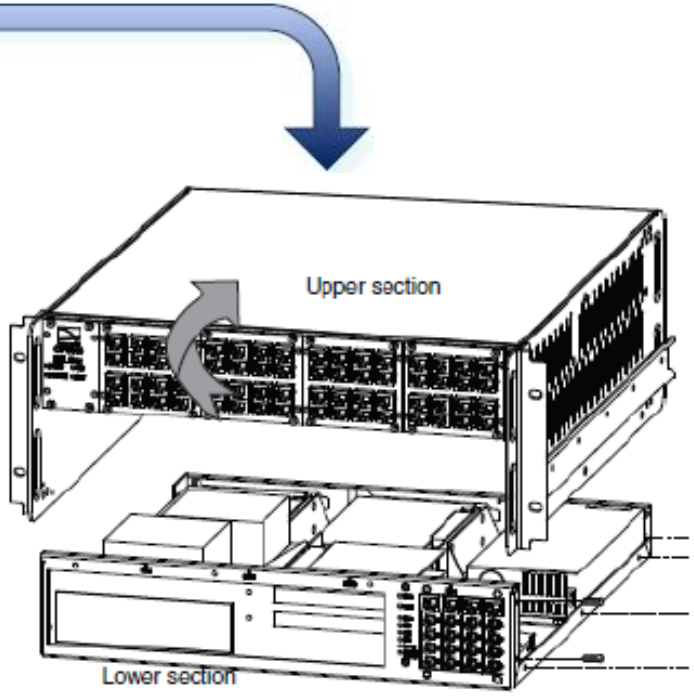
- IEC 61850
- Async TCP/IP, Serial
- CAN Bus protocol, MIL 1553
- Aeronautical Radio INC. (**ARINC**); Digital Information Transfer System

OP5600 Hardware Overview

- Upper/Lower Section

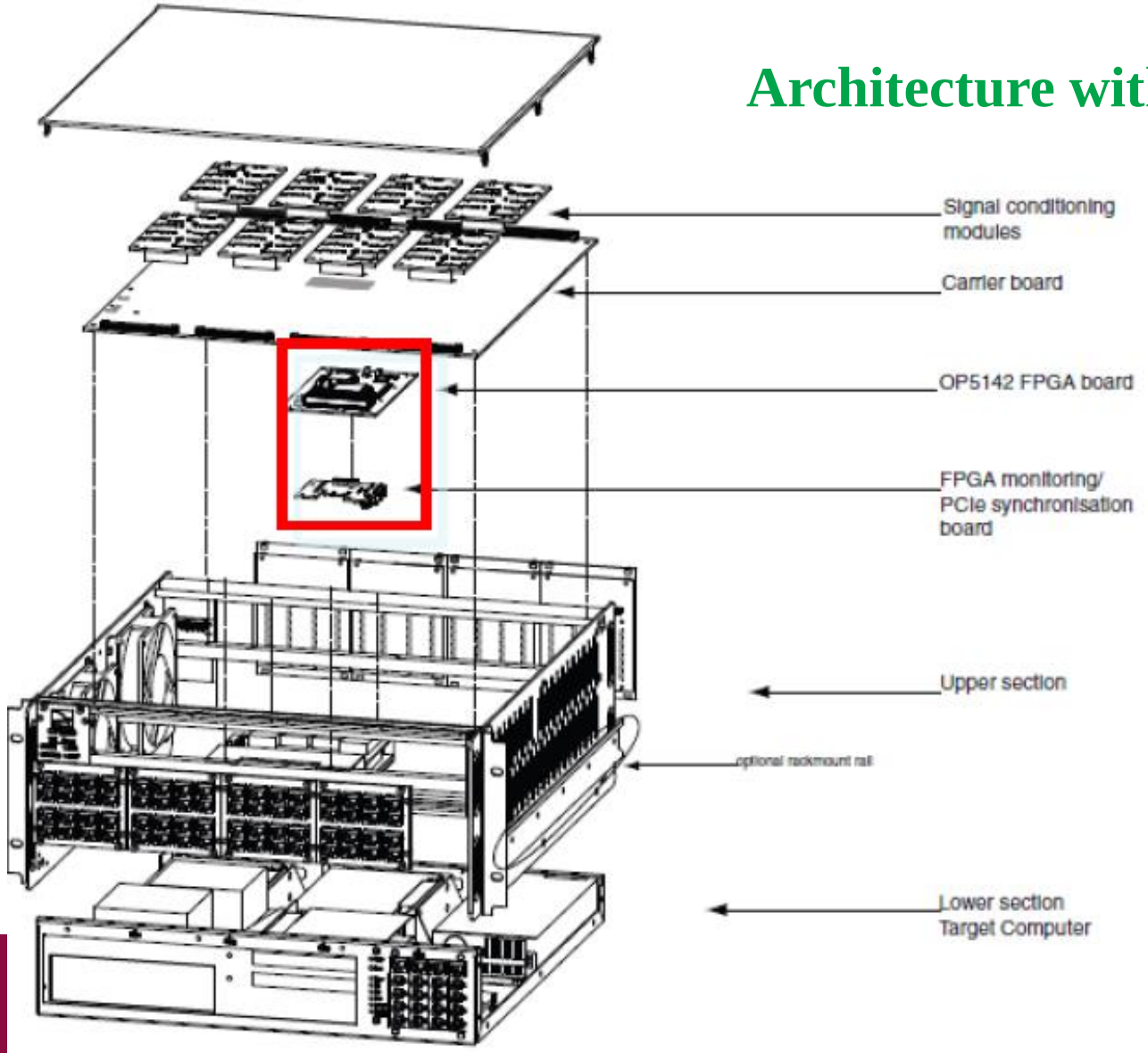
Upper section : ***FPGA and I/O modules*** (analog and digital mezzanines)

Lower section : ***target*** (motherboard, CPUs, RAM, Hard Drive, PCI slots)



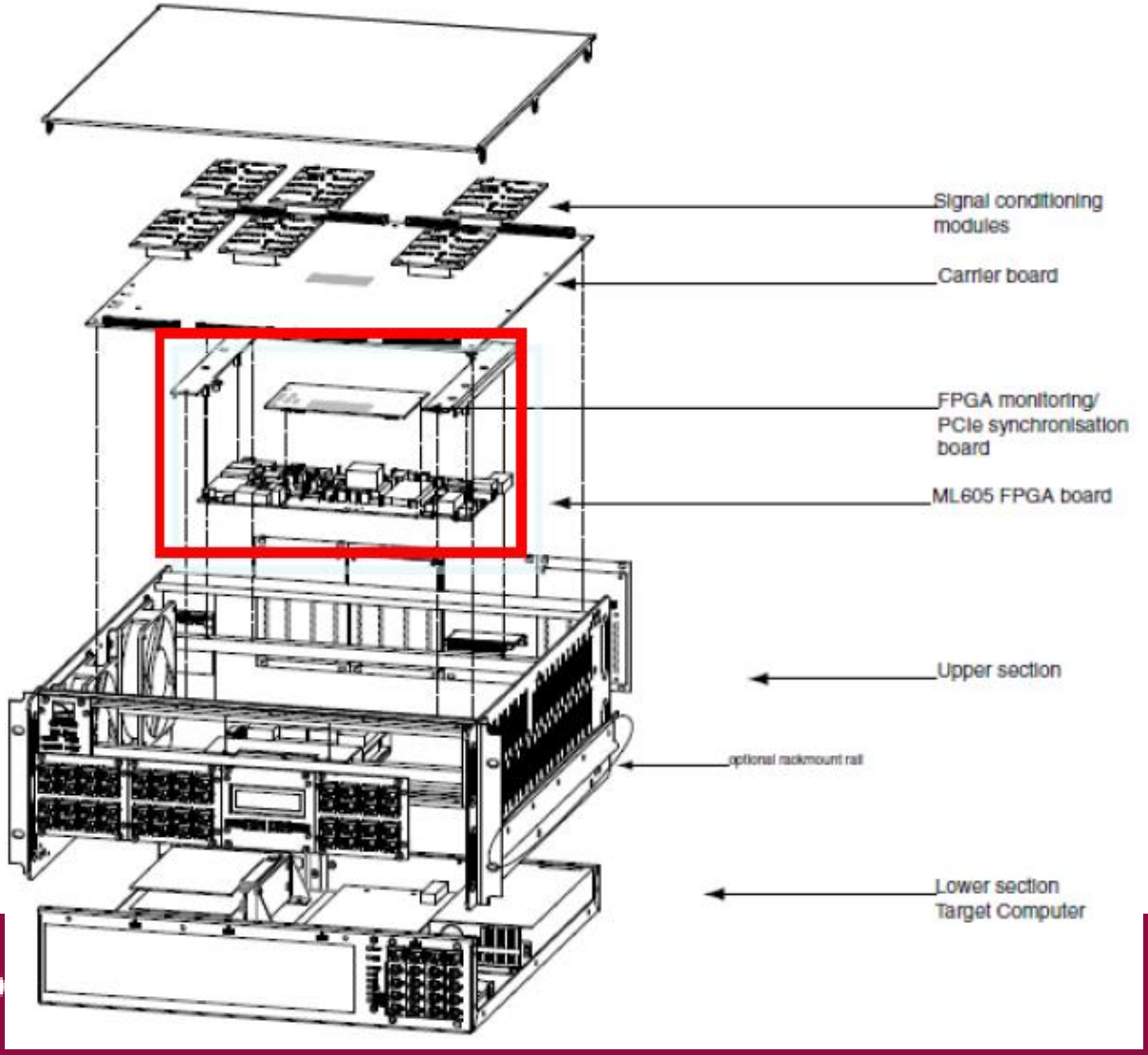
OP5600 Hardware Overview

Architecture with XILINX OP5142



OP5600 Hardware Overview

Architecture with XILINX ML605 (Virtex 6)



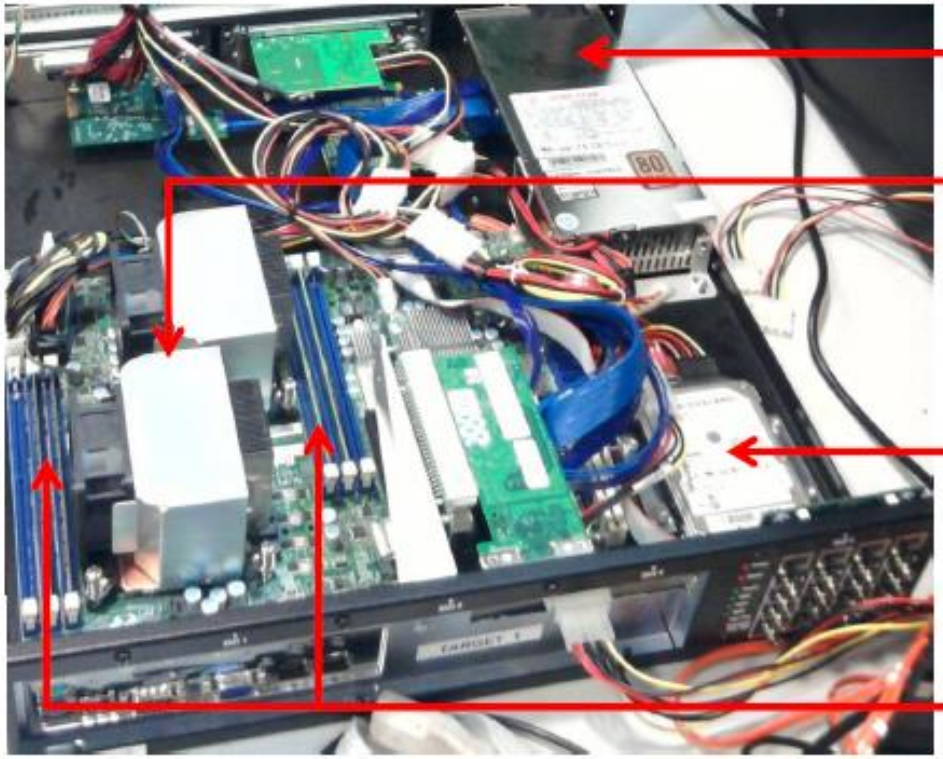
OP5600 Hardware Overview

FPGA ML605, XILINX Virtex 6

- The I/O interface has 6 configurable groups (either 32 digital I/O lines or 16 analog I/O lines).
- High flexible solution: possibility of having different IO combinations with the same FPGA board.
- up to 192 Digital I/Os or up to 96 16-bit ADC and DAC channels
- Sampling time : 100 MHz or 200 MHz

OP5600 Hardware Overview

Lower section : target

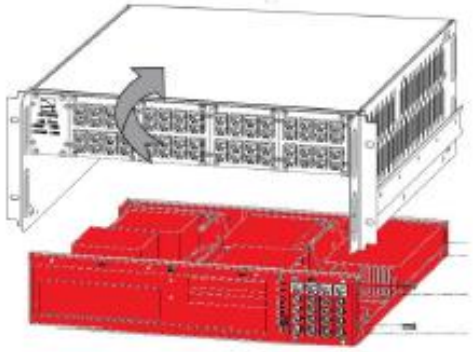


Power supply

CPUs *(this is where the models are executed)*

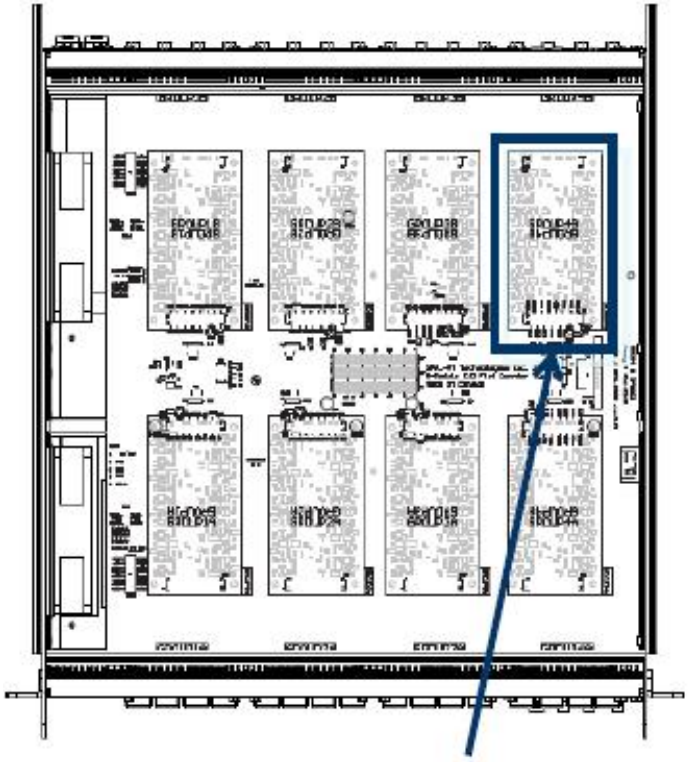
Hard Drive *(to store models and logged files)*

RAM

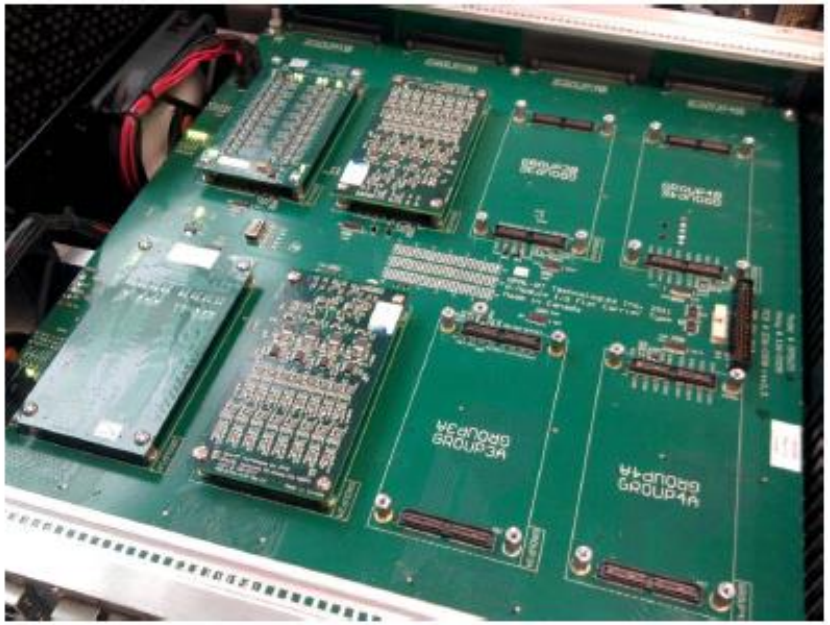


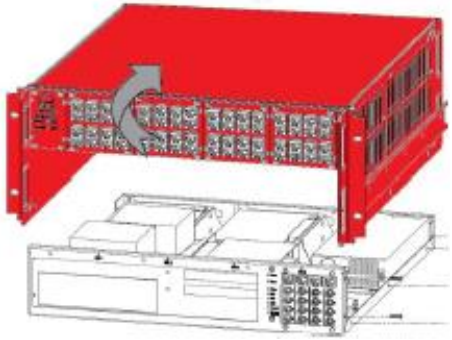
OP5600 Hardware Overview

Upper section : I/O modules



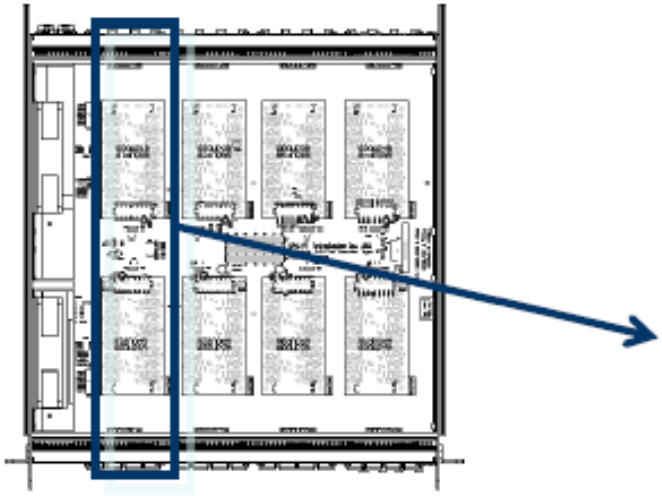
I/O Conditionning module
(mezzanine)





OP5600 Hardware Overview

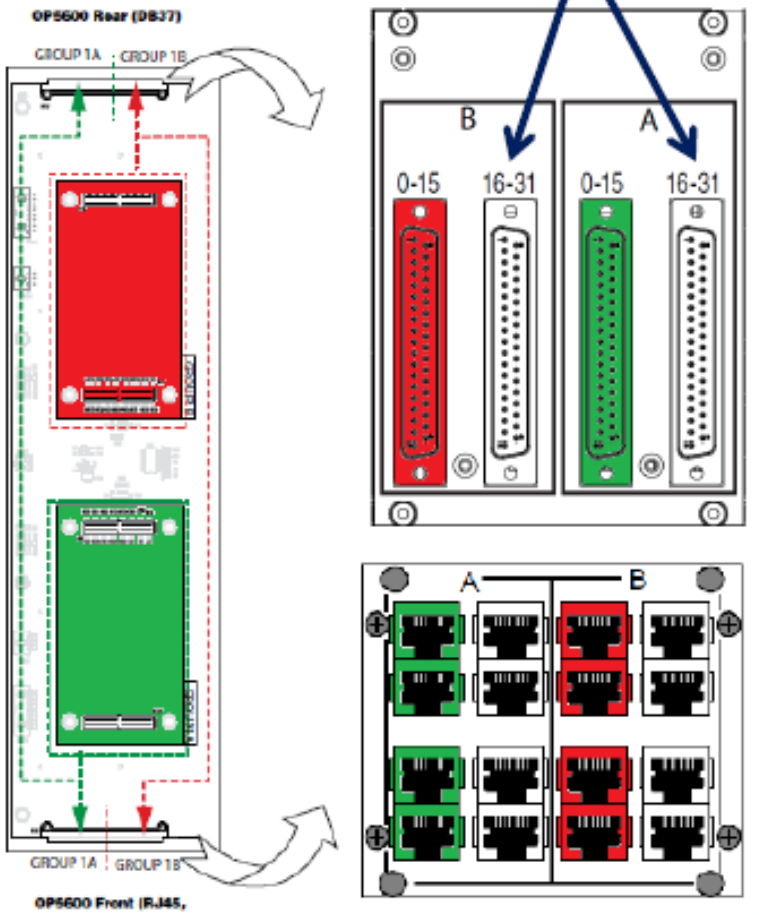
Analog mezzanines



16 channels per mezzanine

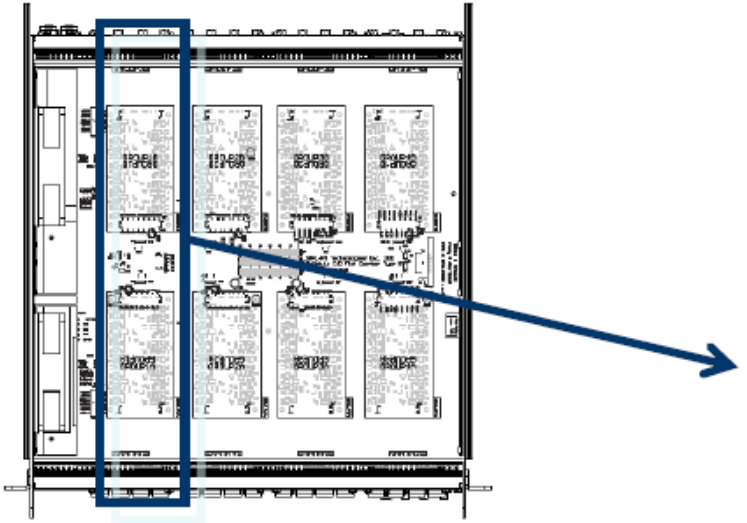
- OP5330 : 16 analog out
- OP5340 : 16 analog in

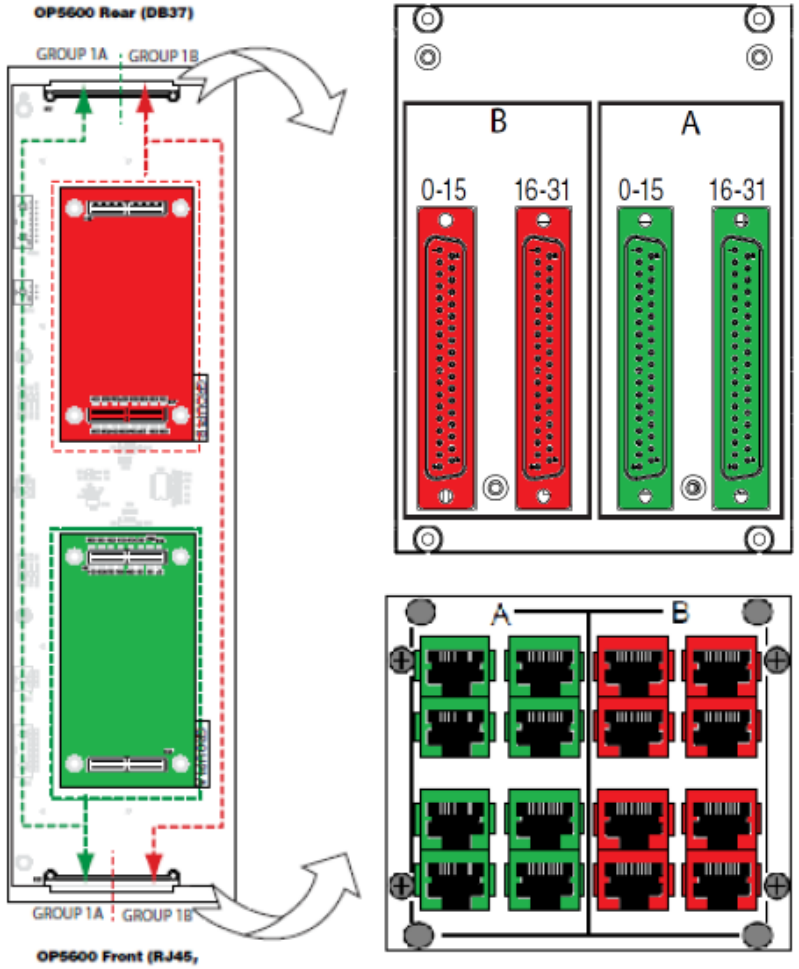
Channels 16 to 31 are not used



OP5600 Hardware Overview

Digital mezzanines

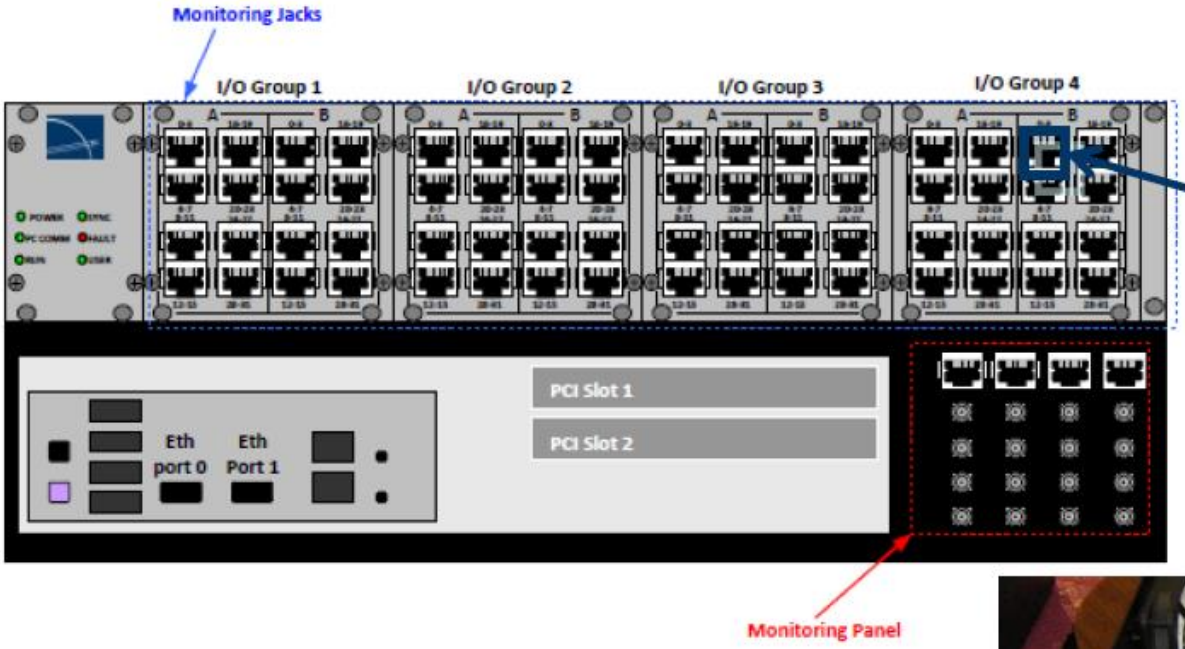




32 channels per mezzanine

- OP5353 : 32 digital in
- OP5354 : 32 digital out

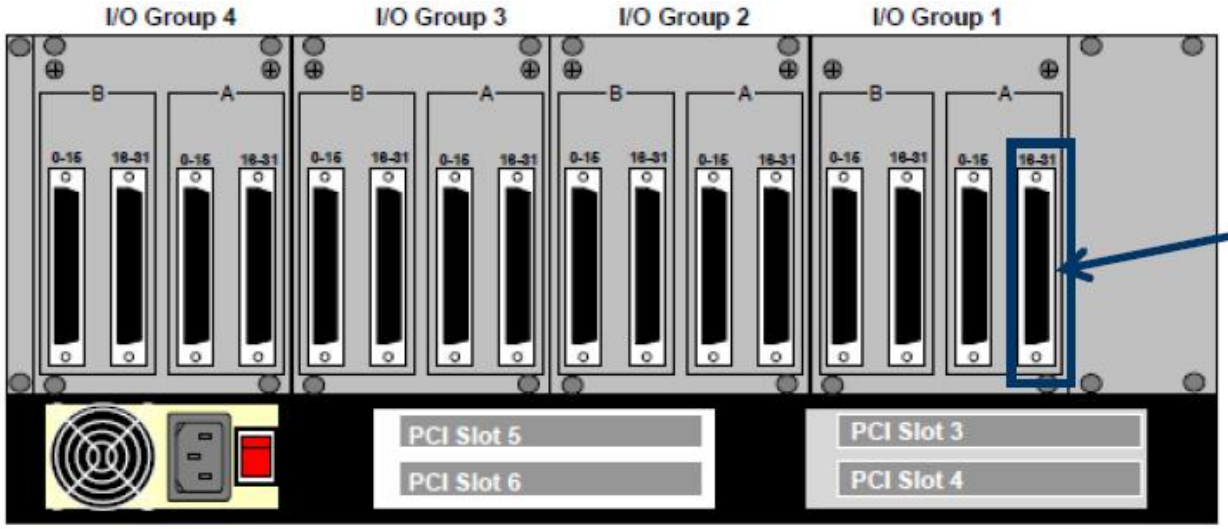
Front View



One RJ45 connector drives 4 signals

The front view is used for monitoring purposes only

Rear View



One DB37 connector drives 16 signals

The rear view is used to connect external hardware to the OP5600

Simulink I/O Blocks

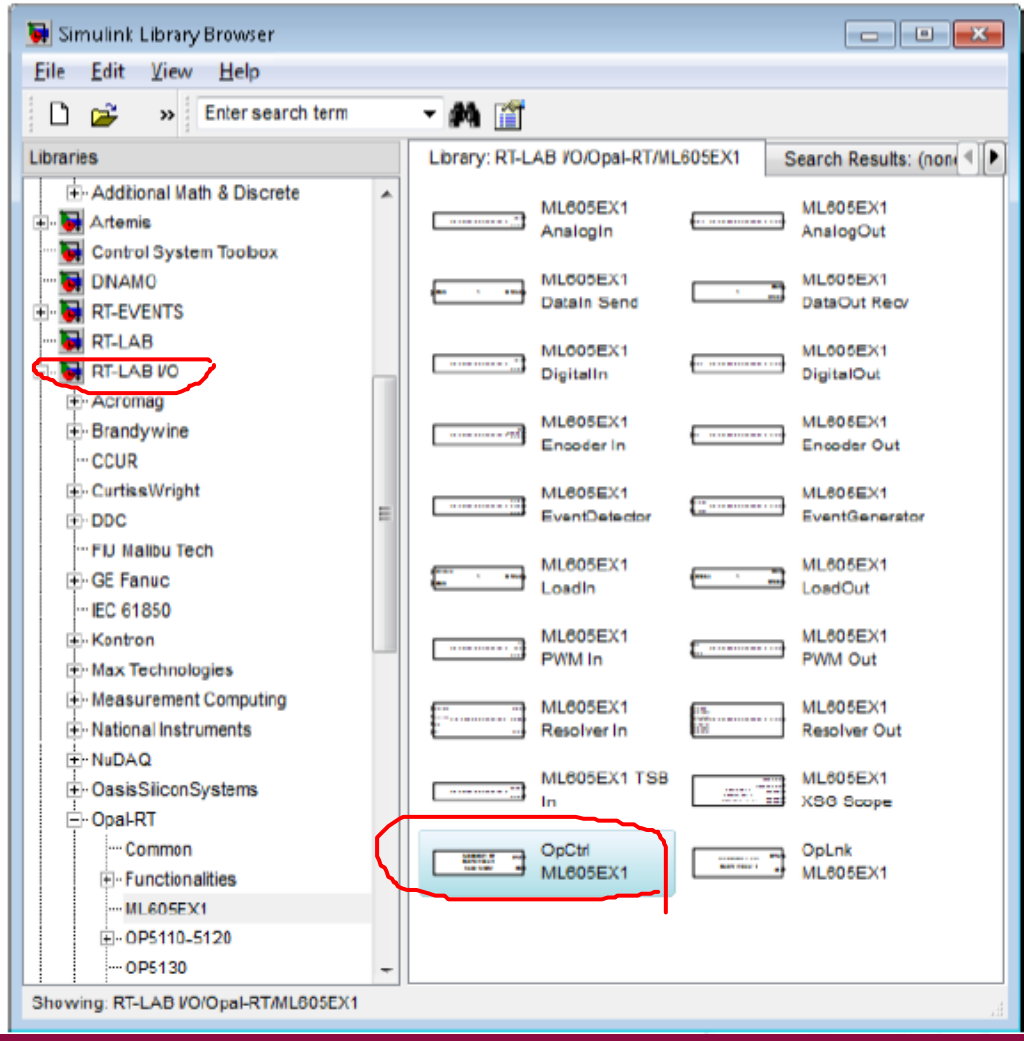
OP5142 & ML605 FPGA boards allow to drive the analog and digital I/O cards located in the simulator:

- Analog Input & Output
- Static Digital Input & Output
- Time-Stamped Digital Input & Output
- Encoder Out & Encoder In (Decoder)
- TSB In
- Etc...

All those I/O blocks can be found within the same library:

RT-LAB I/O > Opal-RT > OP5142EX1

RT-LAB I/O > Opal-RT > ML605EX1

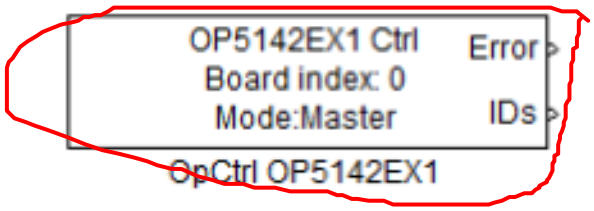


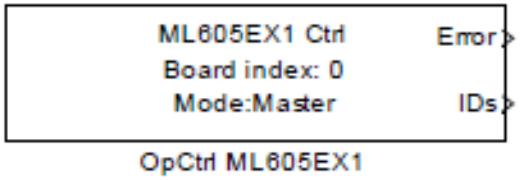
Simulink I/O Blocks and Configuration

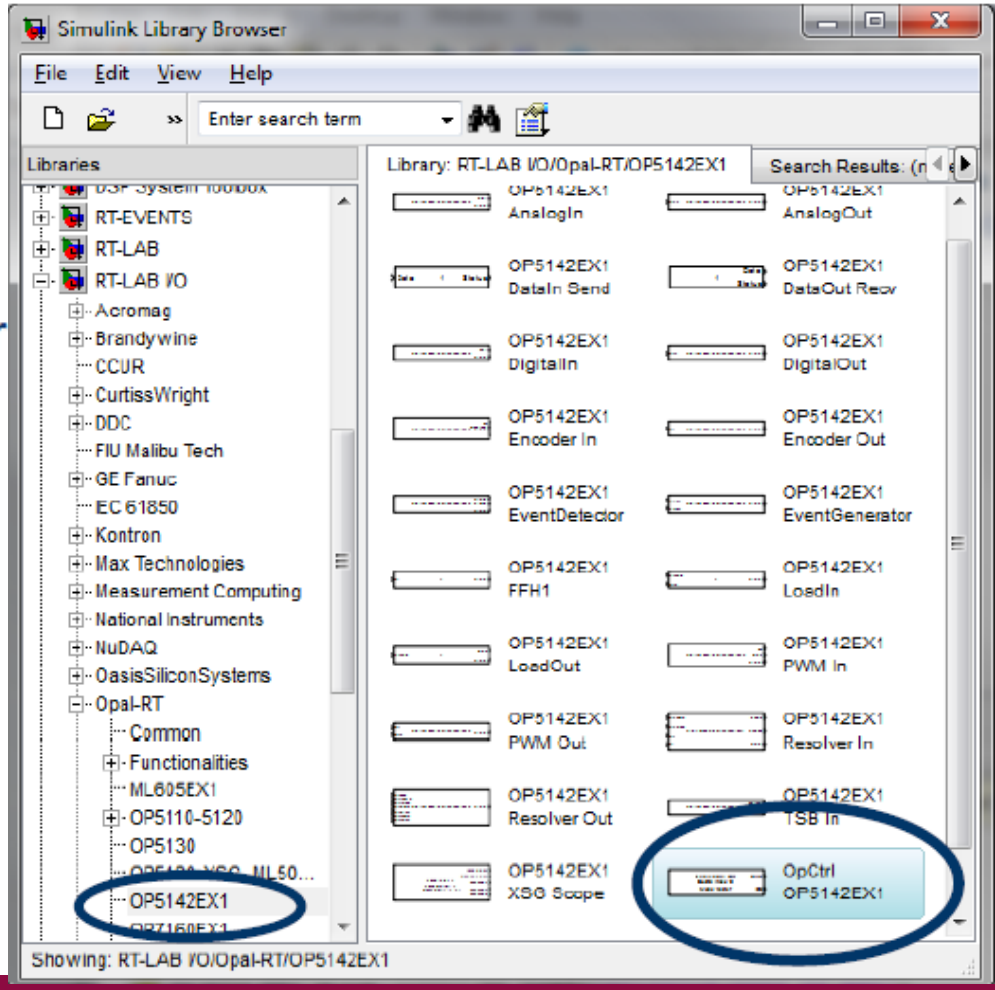
Simulink FPGA Controller Block

- OpCtrl Block
  - Handles synchronization
  - Set Internal Parameters

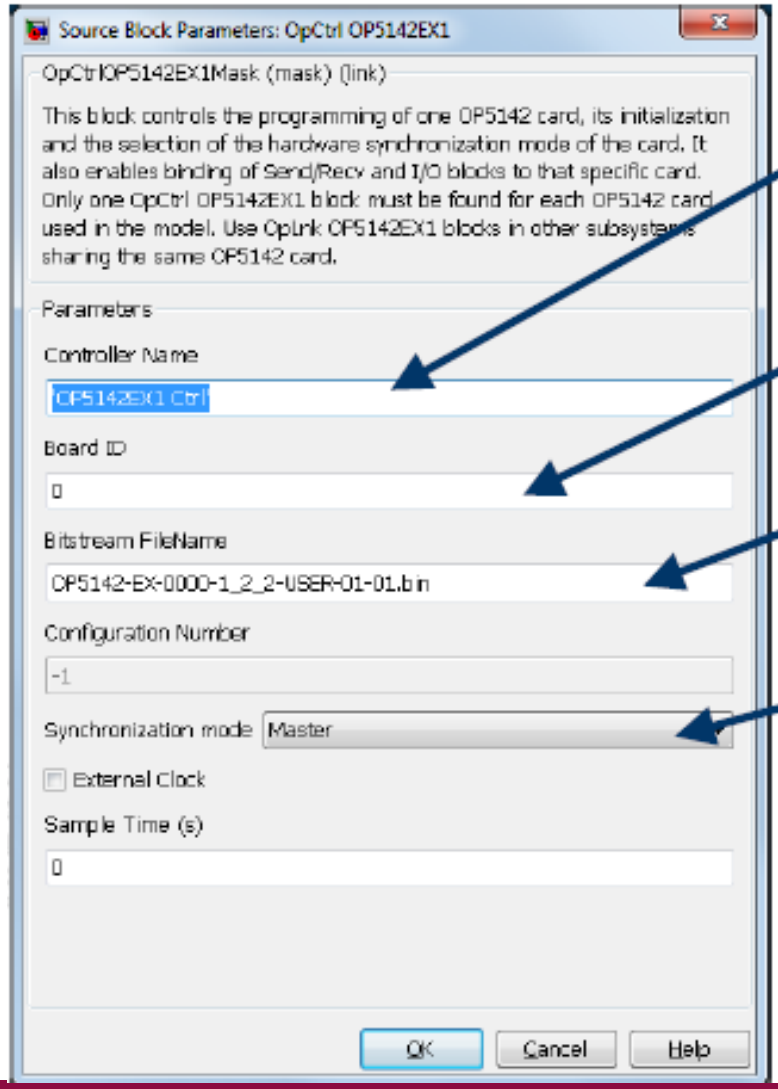
- Block must be inserted in model for each FPGA board that is physically present in your system



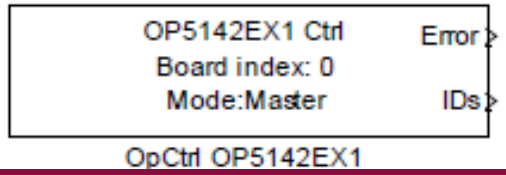


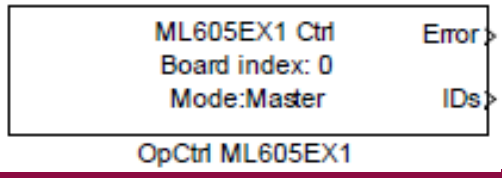


OpCtrl Block – Internal Parameters

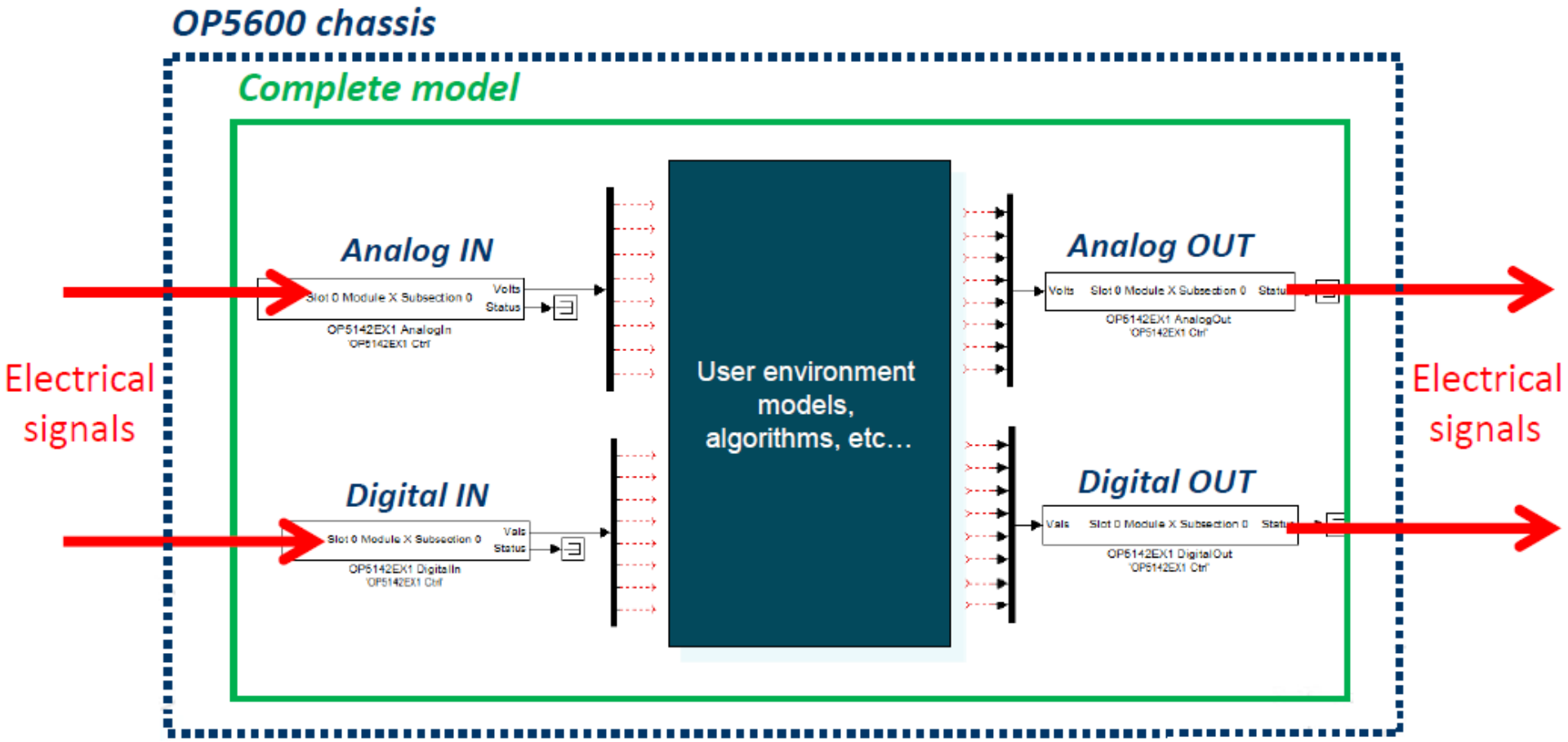


- Label for the controller block *(can be changed)*
- Board index given by the ***Get I/O infos*** command
- Bitstream Filename can be found in System Integration document
- Set to "Master" by default. Set to "Slave" in another FPGA is already defined as "Master"





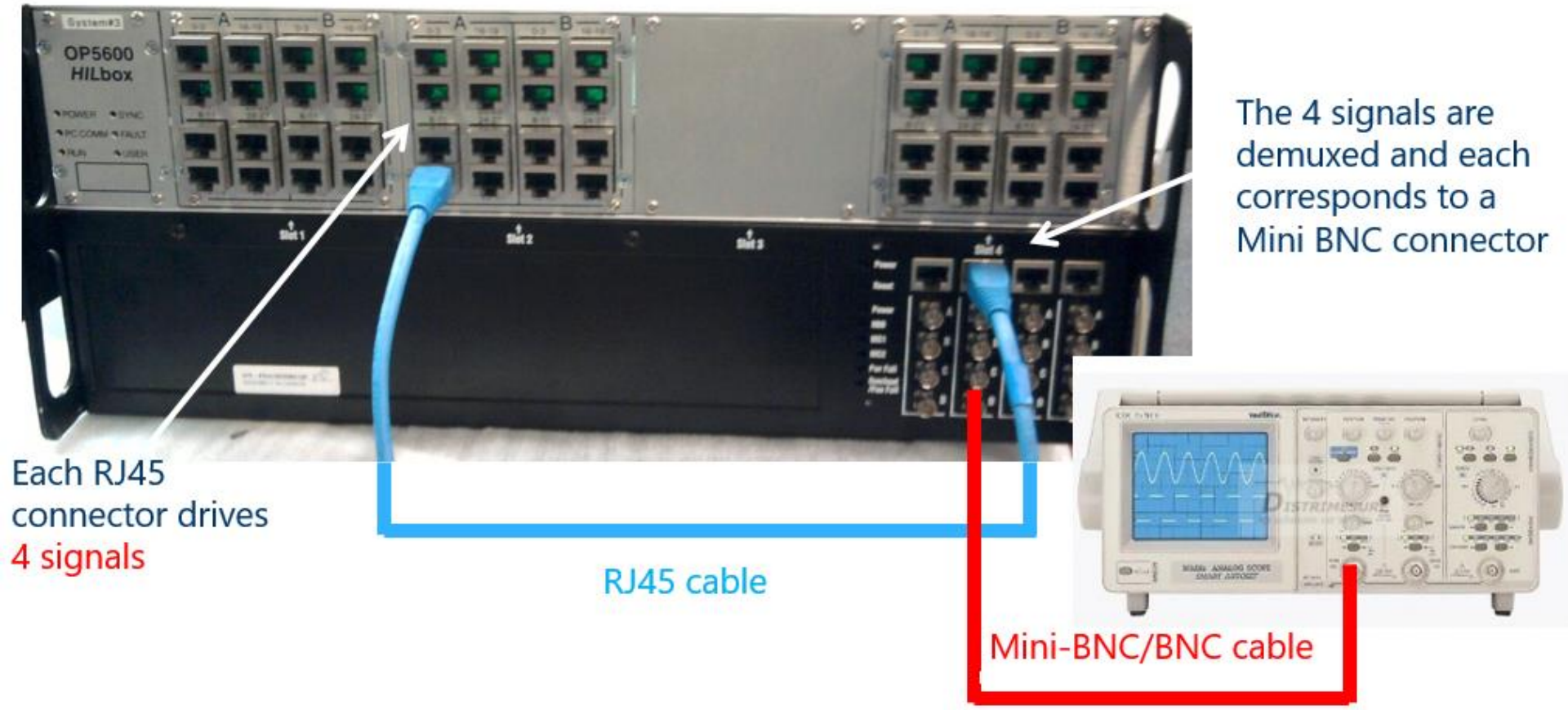
Principle of Inputs and Outputs



Measuring Signals

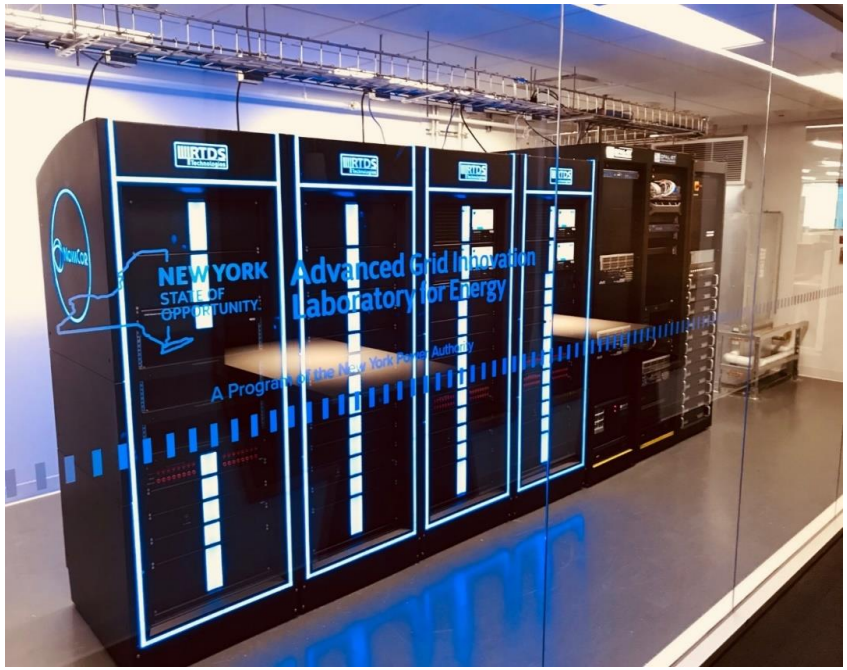
External scope

- The front panel allows the measuring of any input or output signal, before connecting to external hardware

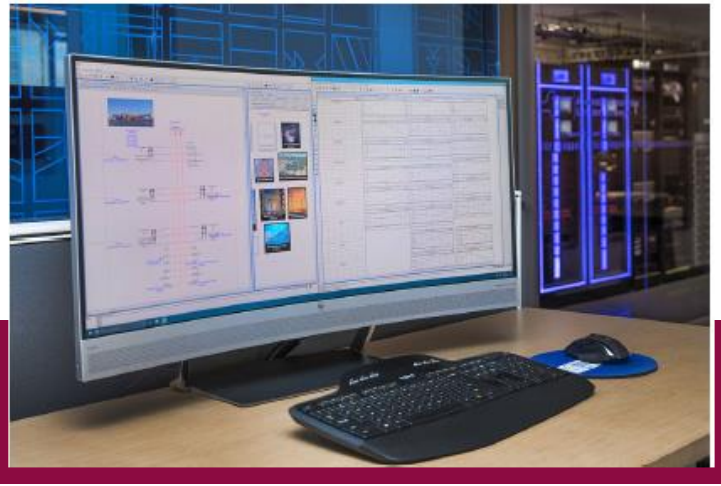


Real-time Implementation: An Example

NY Advanced Grid Innovation Lab for Energy (AGILe)



End-to-end Energy Systems modeling and real-time simulation



OPAL-RT Bootcamp

Real-Time PV System and Battery Simulation Modeling

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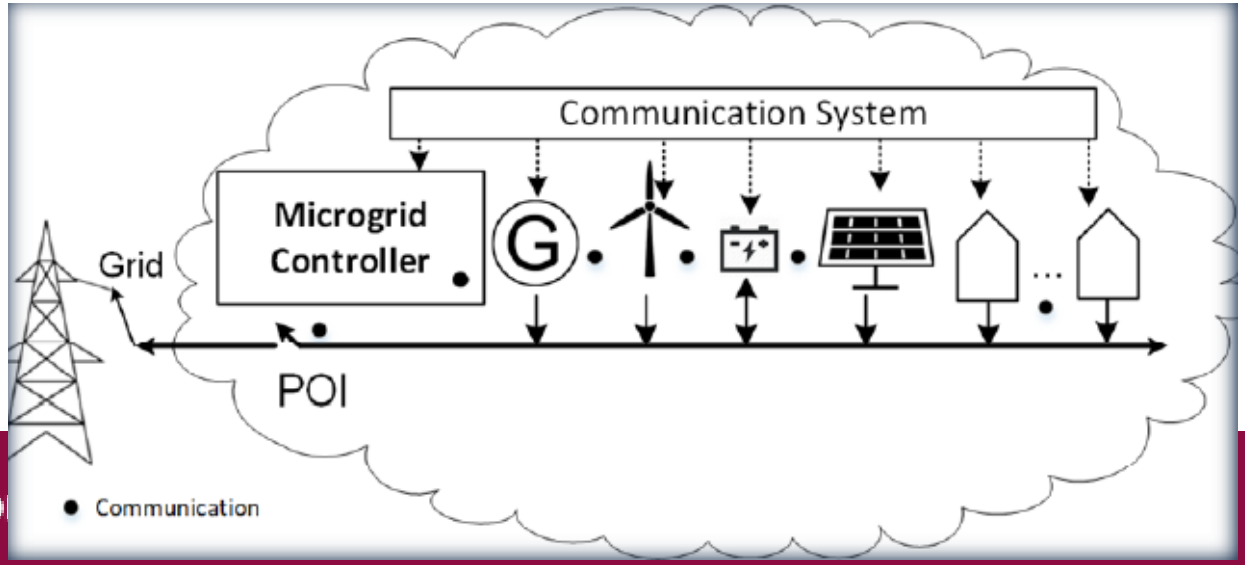
December 18, 2020

Modeling Challenges

- The proliferation of Solar, Wind, Battery storage has given rise to new challenges in power systems operation.
- Energy storage systems are emerging as a potential solution to such challenges.
- To understand their potential and limitations, it is crucial to model and simulate such PV and storage systems with accuracy and high fidelity in real-time fashion.



Related Works

- Multiple PV cells are connected in series or parallel connections to create a PV module, which meets required output voltage and current specifications.
- It is also observed that, Li-ion batteries are the most widely used energy storage devices across all such industrially available ESS.
- Call for fast and accurate modeling of Li-ion batteries for monitoring and control of their charging and discharging modes.

Related Works

- A simplified and efficient model for PV System is shown suitable for real-time simulation.
- Comparisons between the proposed model and the existing model provided by MathWorks W.r.t hardware usage and efficiency are presented.
- Power system operations are time-critical in nature, it is important to test the real-time compatibility of the proposed models to utilize in development, implementation and testing of different control schemes.

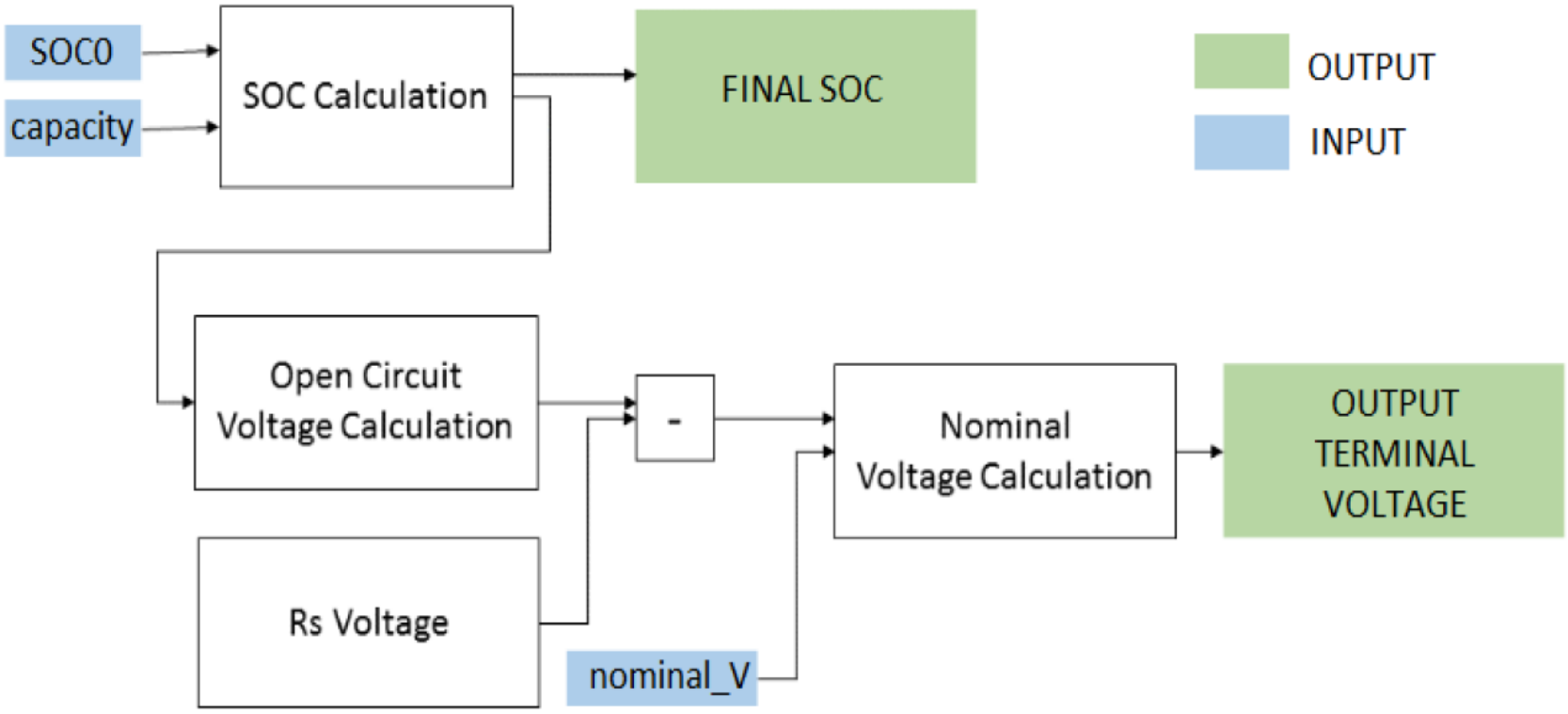
Existing Battery Models

- MathWorks also provides an accurate and detailed generic battery model, which can model four types of rechargeable batteries.

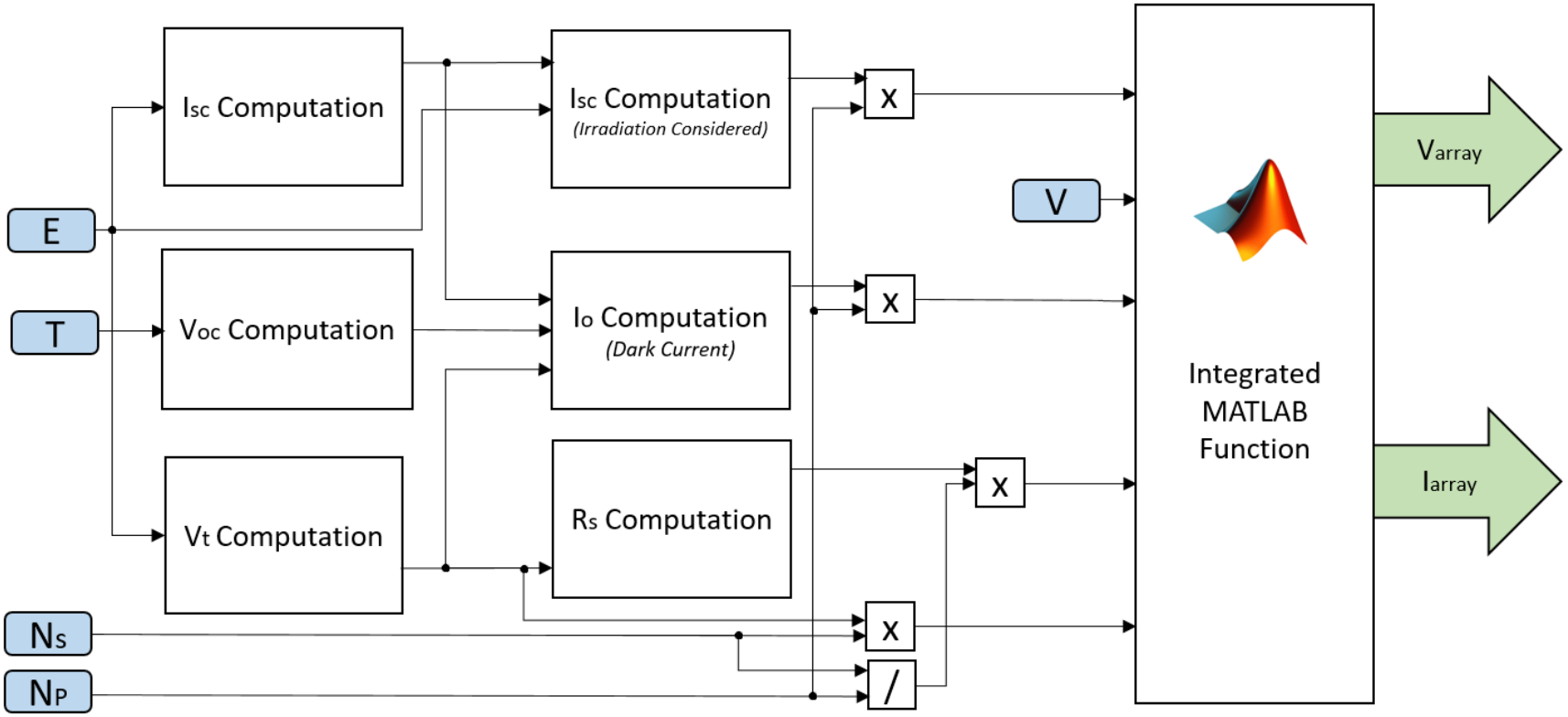
- MathWorks model is suitable for off-line simulations and was used as a benchmark of the model in this assessment.

- Test the real-time performance of the proposed PV+Battery model using Opal-RT simulator. (cross-platform real-time simulation!)

Flowchart of the proposed model implementation



Block-diagram comprising different units of the model for the PV cell



E = Irridiation
T = Temperature
N_s = No of Series Connected PV Modules in string
N_p = No of Parallel Connected PV Modules in string
V = DC Voltage

Algorithm 1 Calculation of I_{array} and V_{array}

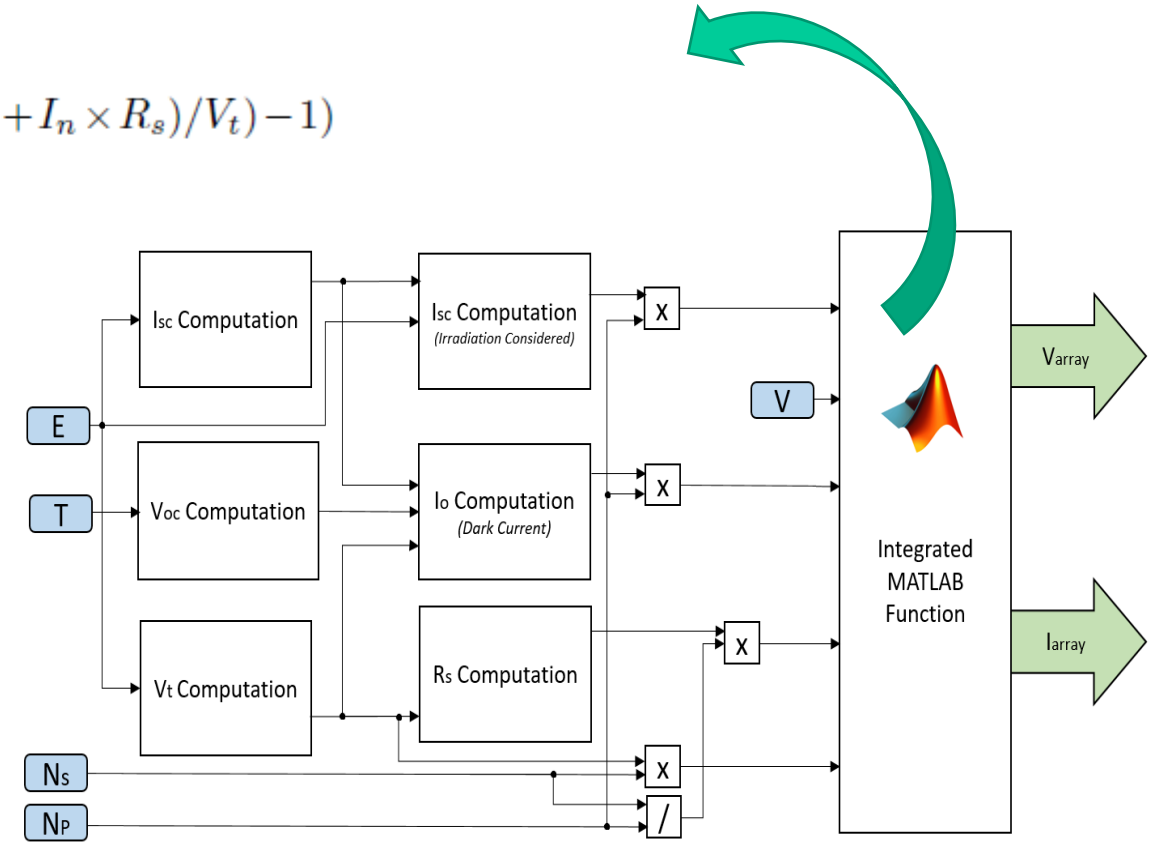
Require: I_{sc}, V_t, N_s, R_s, I_o, V_{DC}

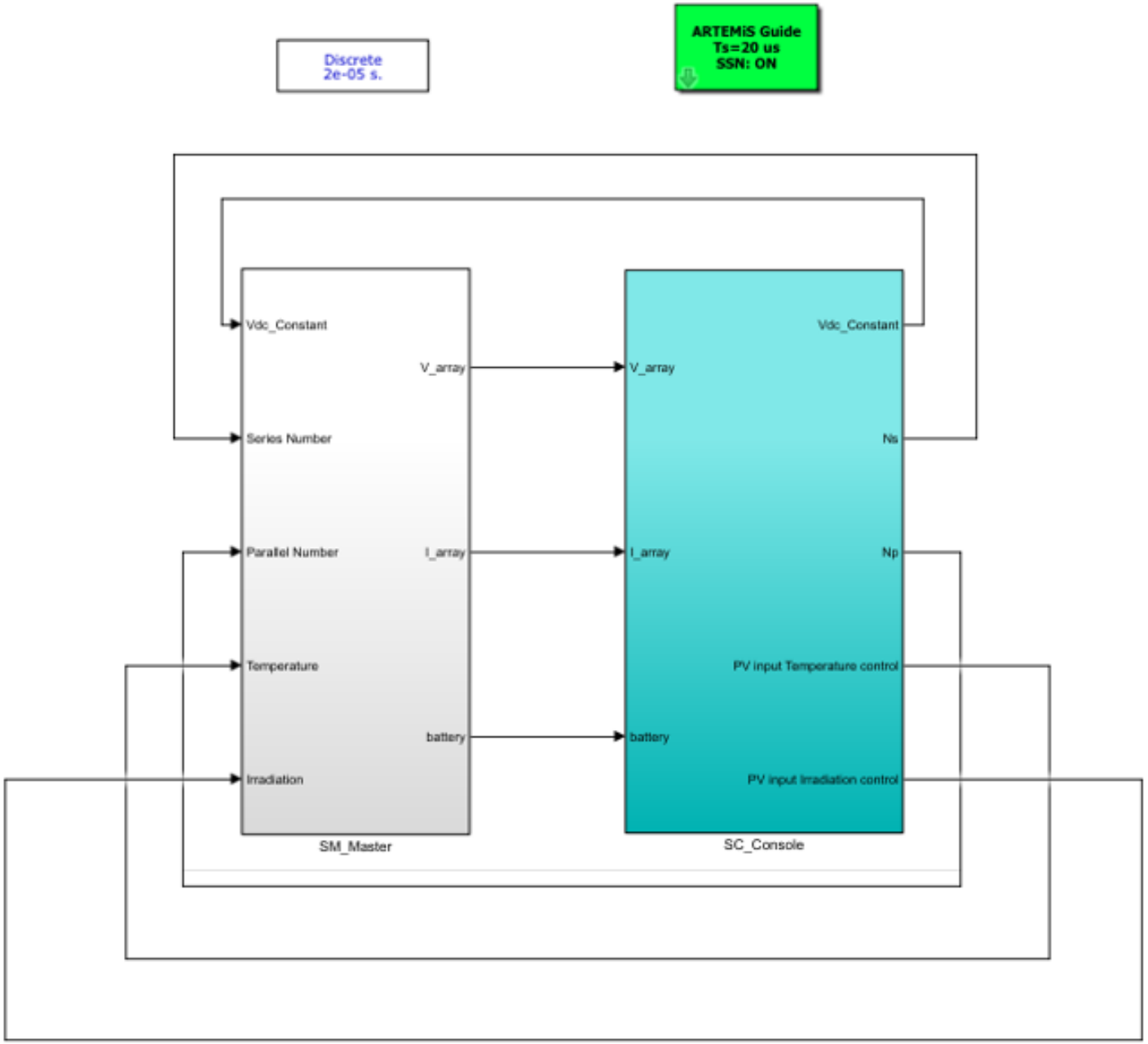
Require: Define:

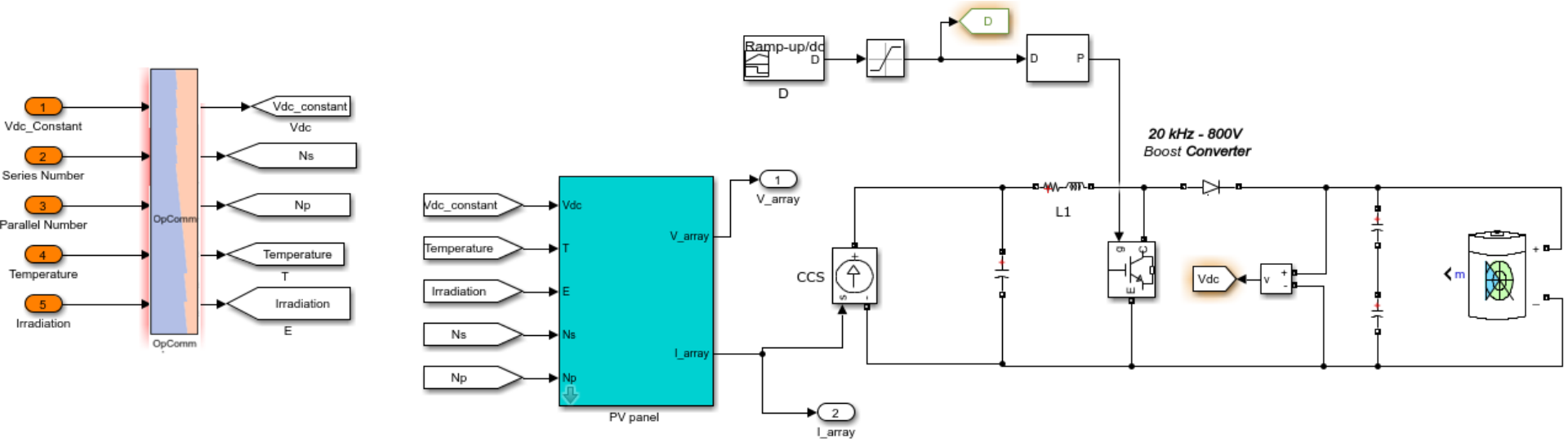
$f(I_n) = I_n - I_{sc} + I_o \times ((exp(V_{DC}/N_s + I_n \times R_s)/V_t) - 1)$

Ensure: $I_{start} = 0$, $e = 10^{-3}$, $L = 0$

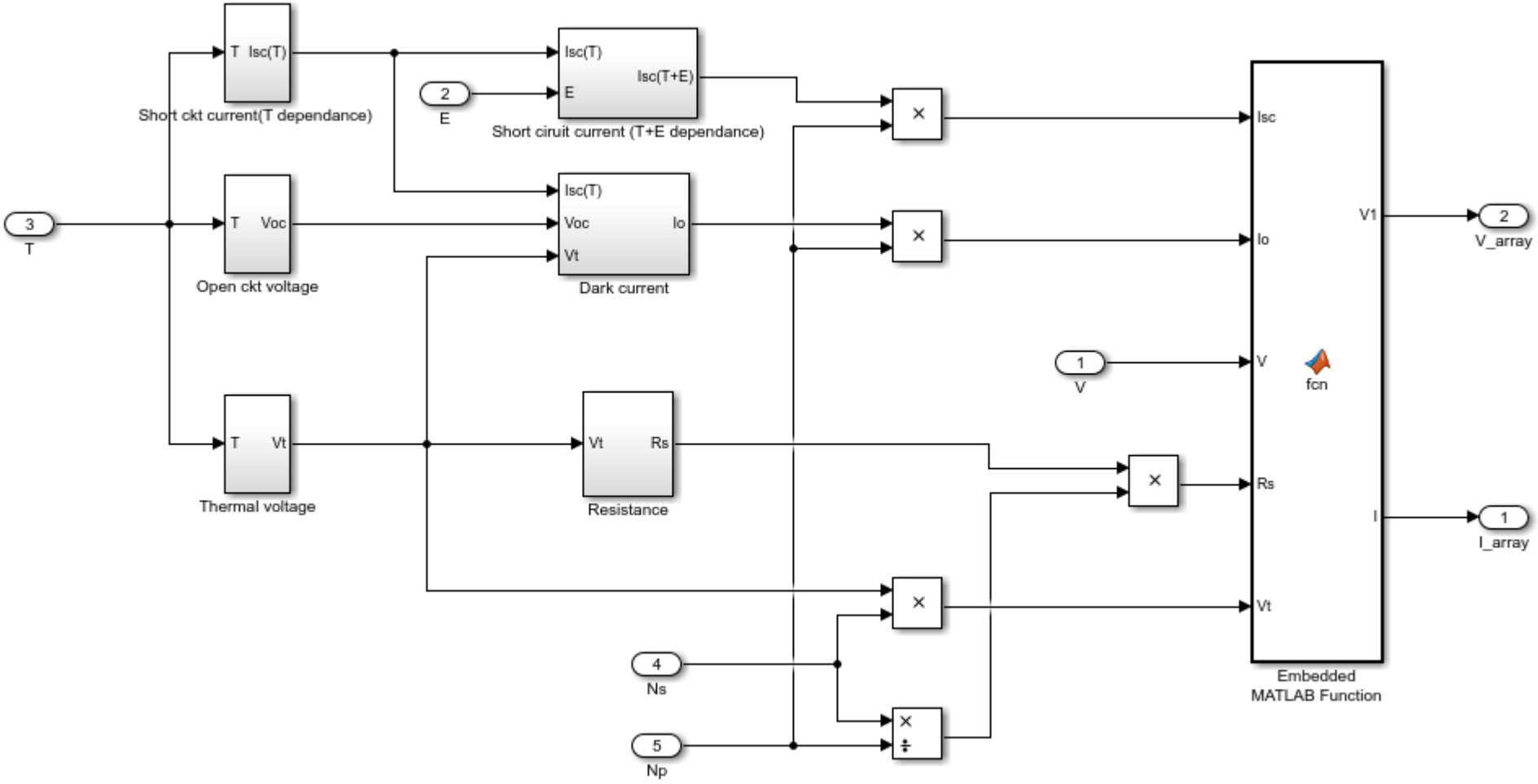
```
while L ≠ 1 do
  if n = 0 then
    I_n = I_start
  else
    n++
    I_n = I_{n-1} − f(I_{n-1})/f'(I_{n-1})
    e_n = I_n − I_{n-1}
    if | e_n | ≤ e then
      I_array ← I_n
      L = 1
    end if
  end if
  V_array ← V_DC/N_s
end while
```

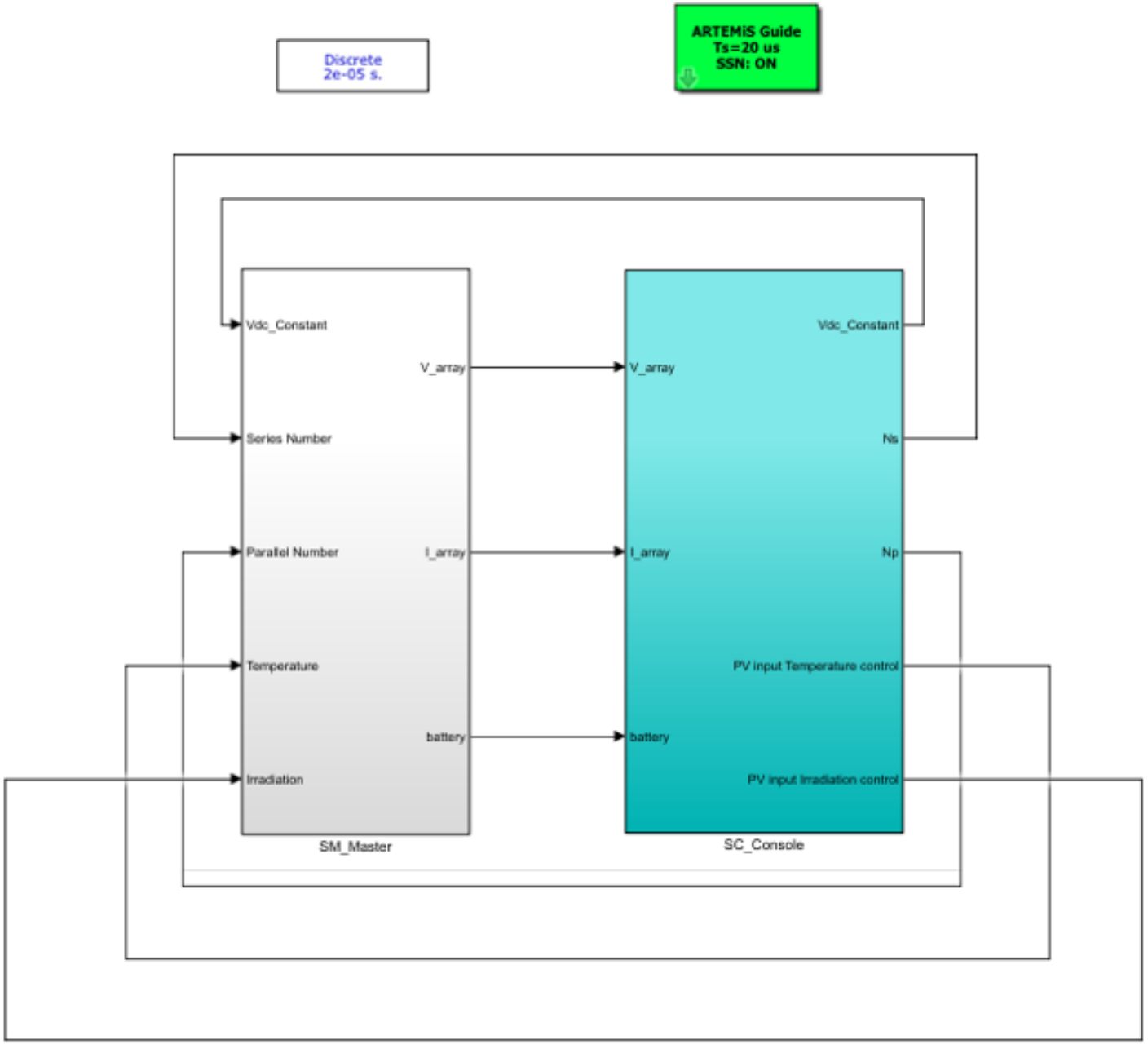


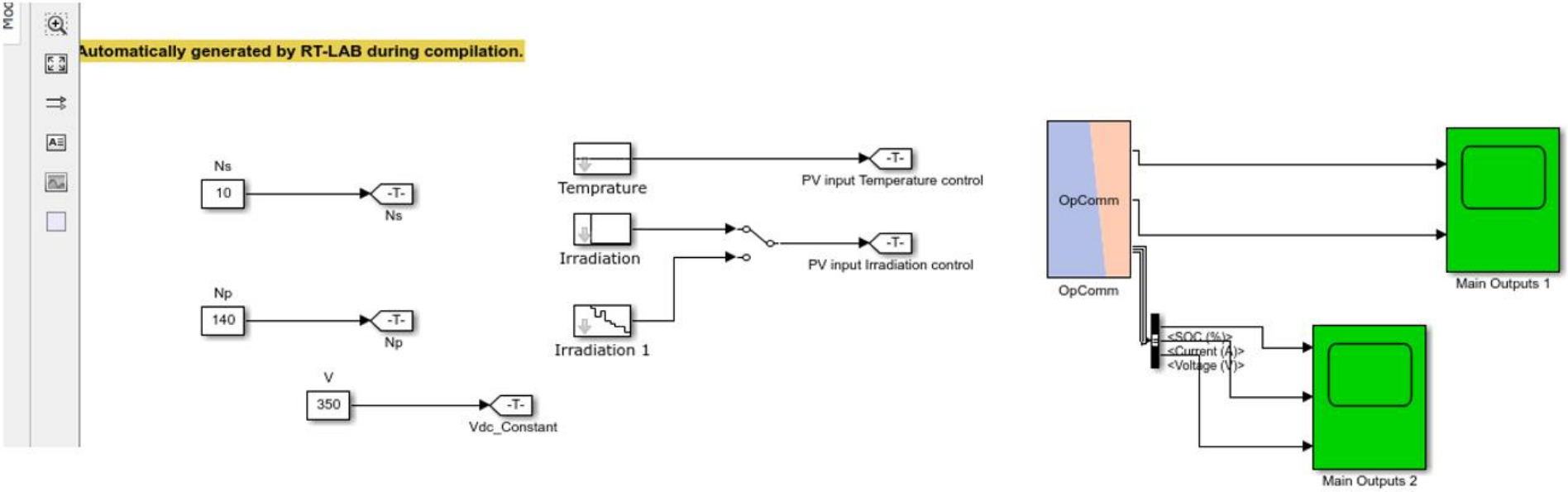

Discrete
2e-05 s.
ARTEMiS Guide
Ts=20 us
SSN: ON
Vdc_Constant
V_array
Series Number
Parallel Number
I_array
Temperature
battery
Irradiation
SM_Master
Vdc_Constant
V_array
Ns
I_array
Np
PV input Temperature control
battery
PV input Irradiation control
SC_Console


1
Vdc_Constant
2
Series Number
3
Parallel Number
4
Temperature
5
Irradiation
OpComm
OpComm
Vdc_constant
Vdc
Ns
Np
Temperature
T
Irradiation
E
Ramp-up/dc
D
D
D
P
D
20 kHz - 800V
Boost Converter
Vdc_constant
Temperature
Irradiation
Ns
Np
Vdc
T
E
Ns
Np
V_array
I_array
PV panel
1
V_array
2
I_array
CCS
L1
Vdc
v
m

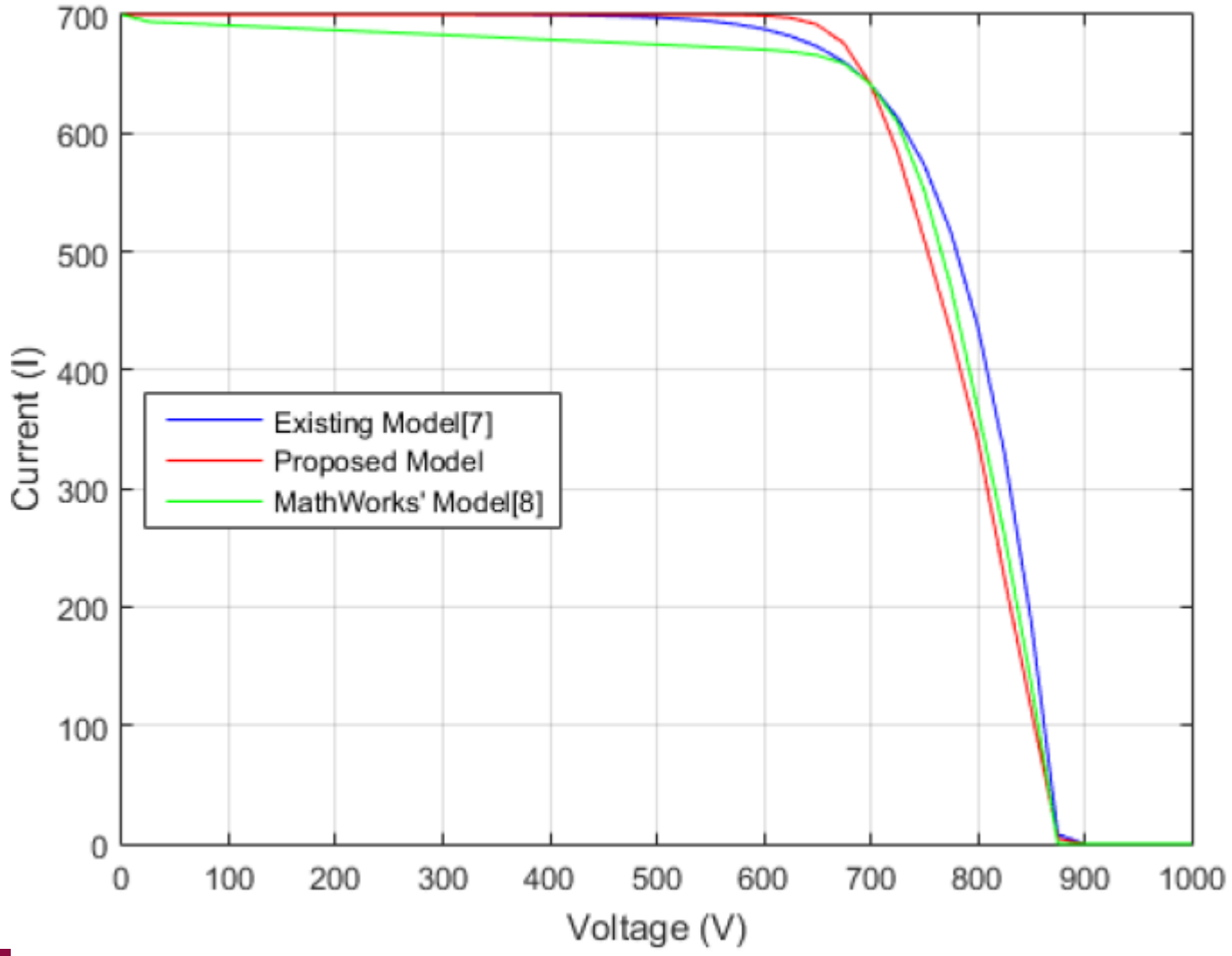
Block-diagram comprising different units of the PV cell model implementation



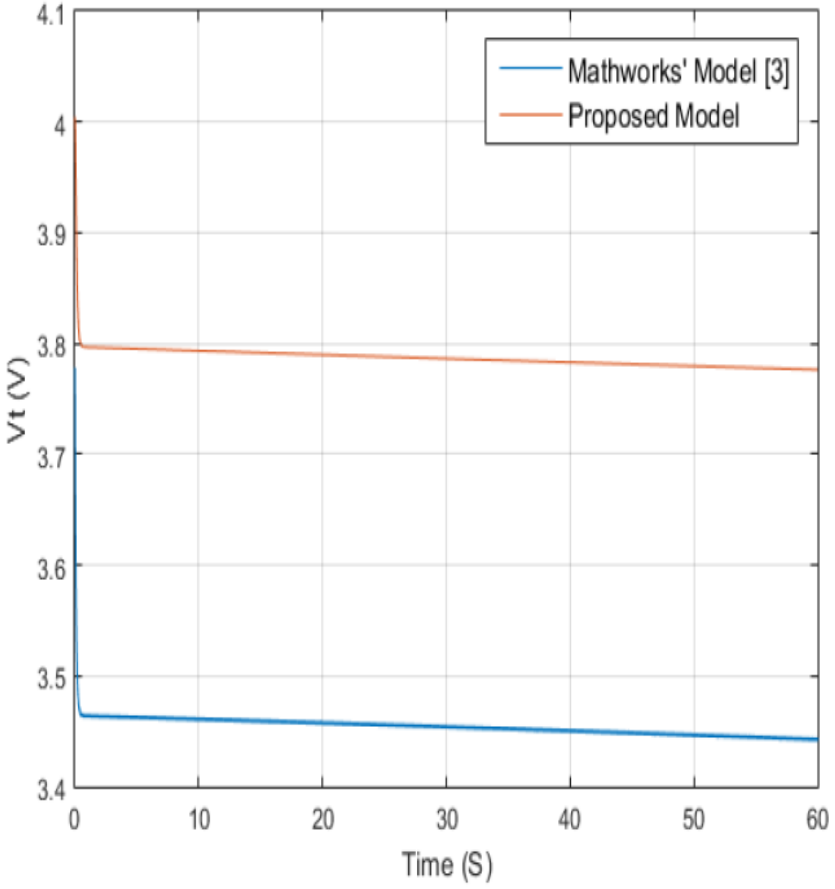

Discrete
2e-05 s.
ARTEMiS Guide
Ts=20 us
SSN: ON
Vdc_Constant
V_array
Series Number
Parallel Number
I_array
Temperature
battery
Irradiation
SM_Master
Vdc_Constant
V_array
Ns
I_array
Np
PV input Temperature control
battery
PV input Irradiation control
SC_Console

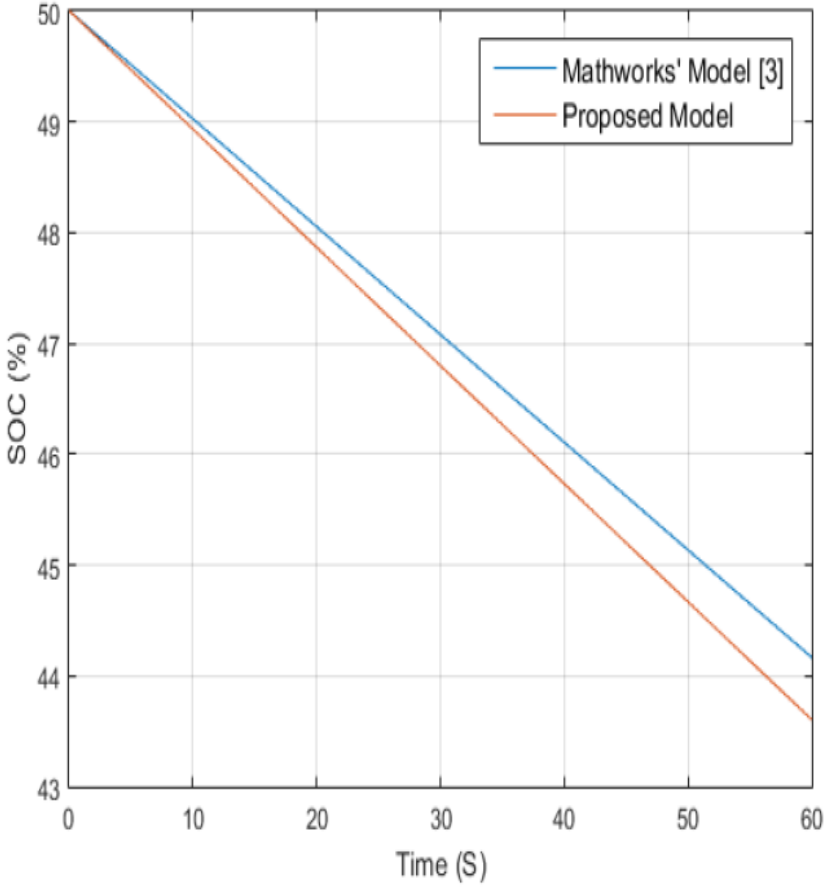

Automatically generated by RT-LAB during compilation.
Ns
10
-T-
Ns
Np
140
-T-
Np
V
350
-T-
Vdc_Constant
Temprature
-T-
PV input Temperature control
Irradiation
-T-
PV input Irradiation control
Irradiation 1
OpComm
OpComm
Main Outputs 1
<SOC (%)>
<Current (A)>
<Voltage (V)>
Main Outputs 2

V-I Characteristics of all the PV models



Discharging Mode: Terminal Voltage and SOC variation for the proposed and benchmark models





PERFORMANCE CHARACTERIZATION OF THE PROPOSED PV MODEL IN OPAL-RT PLATFORM

	MathWorks' Benchmark PV Model(A)	Proposed PV Model (B)	Change	Benchmark Model on other platforms
SSN: State Space Operation Count	110	80	-27.27%	Model A is not reproducible in other platforms
SSN: Memory Usage	0.003525	0.002522	-21.21%	
Network Info	8	7	-14.28%	
Computation Time	1.278 us	1.097 us	- 14.48%	

With the simplification of the PV model, the hardware resource requirements for real time simulation on Opal-RT platform reduced.